

APPENDIX A

a

**LM2453**  
**PRODUCT REQUIREMENT SPECIFICATION**  
**V0.17**

NATIONAL CONFIDENTIAL

Andy Morrish 12/24/1998

09698739-102700

**INDEX**

Information contained herein is  
subject to change without notice.

## Monolithic Triple 5.5 nS CRT Driver with Integrated Clamp and G1 Blanking



## External System voltage reference

## 1.0 General Description

The ACDC driver is an integrated high voltage triple CRT driver circuit designed for use in color monitor applications. The IC contains three high gain, differential input, high input impedance, wide band amplifiers which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to -60 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

Integrated with the driver is triple clamp circuit for DC recovery of each of the AC coupled outputs. The DC clamp circuit amplifies the clamp signal that is multiplexed on the video signal input. The DC clamp amplifiers are high gain, differential input, high input impedance amplifiers, setting a low impedance DC level at the clamp output which can be used to restore the DC level of the cathode drive. Each channel has a gain that is internally set to +72.

Also integrated within the package is a 45vp-p vertical blanking driver that is designed to drive the vertical retrace blanking signal to the G1. This is a current limited, low impedance output capable of driving normal G1 decoupling capacitances via an external resistor.

The output of the G1 driver can also be used to drive a voltage boost capacitor (10uF). When connected between the G1 drive output and the 120v supply input pin, a 120v boost supply is achieved which can be used to drive the internal DC clamp circuit, thereby eliminating the requirement for a 120V clamp supply. When the first vertical blanking pulse is received, the G1 drive output enters a current limited latched state until the 120v boost capacitor is fully charged. Thereafter, the G1 output pulses in response to the vertical blanking pulse received on the multiplexed Vref signal line.

The IC is packaged in an industry standard 15 lead TO-220 molded plastic power package.

The input signal interface to the IC is a multiplexed signal containing both clamp and video signal information, relative to an external 1.8v DC reference.

## 2.0 Intended Applications

The ACDC driver has a nominal tr/ff of 5.5ns. With normal amounts of external inductive peaking, this device is targeted for use in applications with pixel clocks up to around 110MHz. This makes the device ideally suited for 1280x1024 at 75Hz. (140MHz pixel clock). Some customers may be able to obtain useful performance up to 160MHz pixel clock, or 1280x1024 at 85Hz., depending upon the individual customers criteria for how much bandwidth is required for a given application.

Target applications running at these speeds are mid range 15" and 17" monitors.

## 3.0 Basic Application Schematic and Connection Diagrams

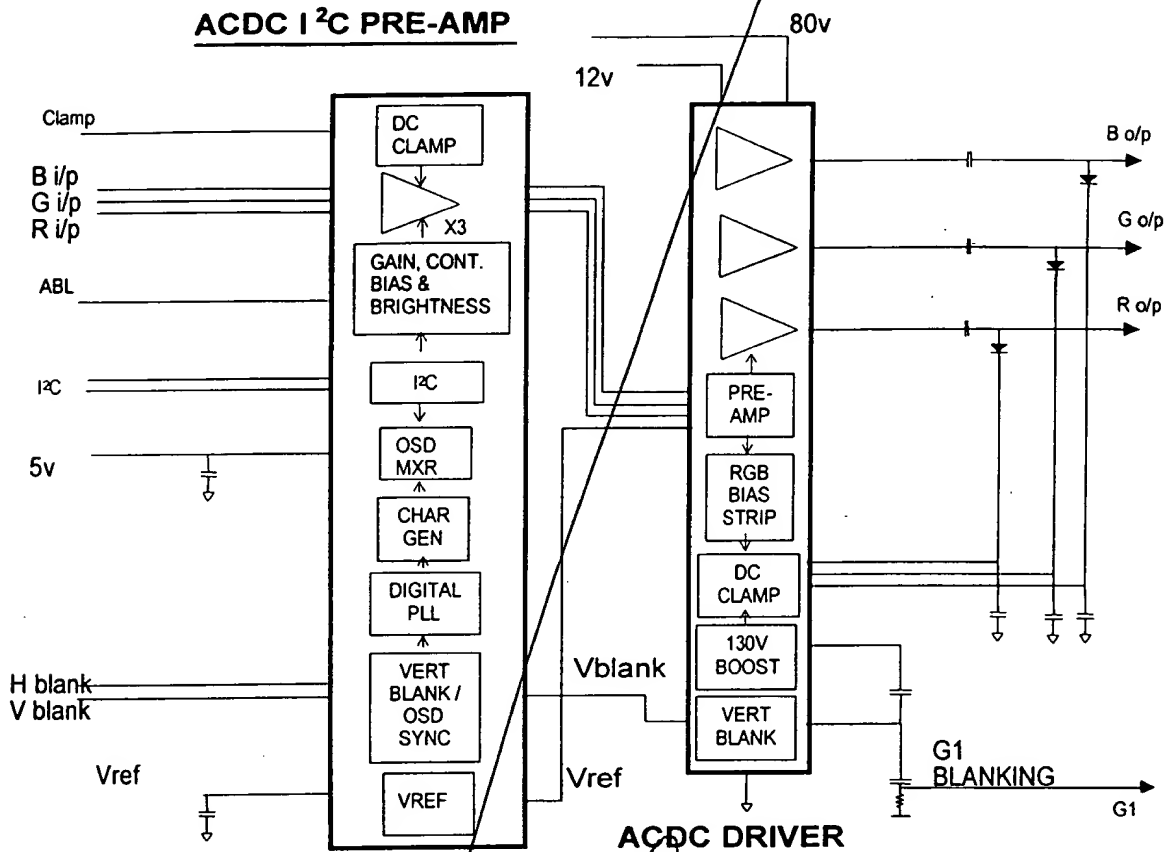


Figure 1. Simplified Schematic Diagram

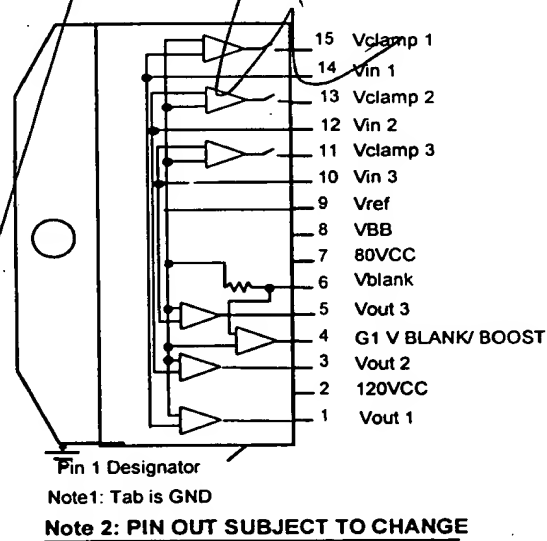


Figure 2. Top View

#### 4.0 Special Features

The ACDC system using the National Video-plex™ multiplexed video signal to send the video signal and DC clamp level from preamplifier to driver. The basic signal scheme is shown in figure 3.

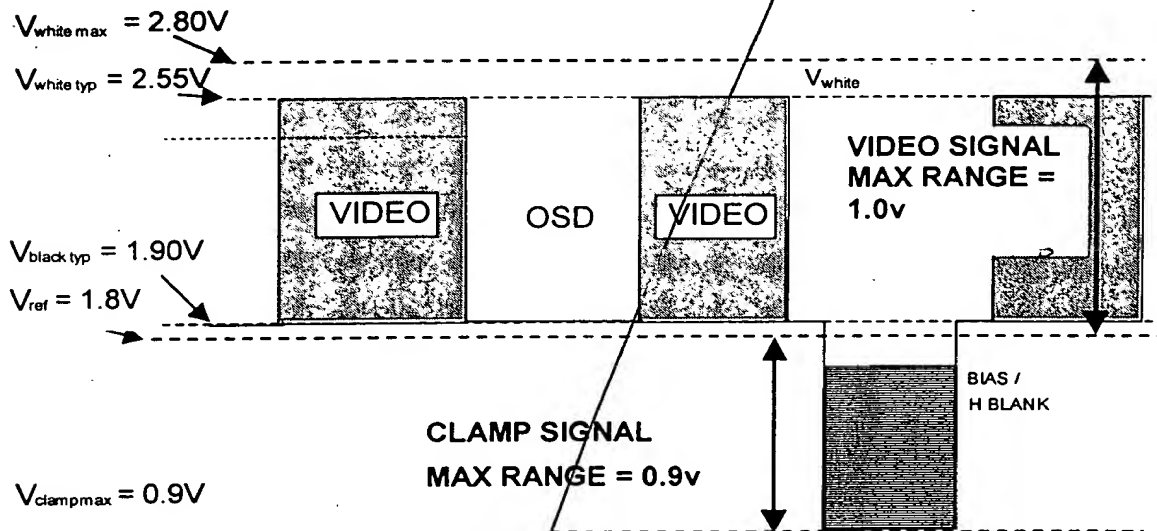


Figure 3. ACDC SYSTEM TYPICAL VIDEO SIGNAL

The response to the video and clamp amplifiers to the video-plex™ signal is shown in figure 4.

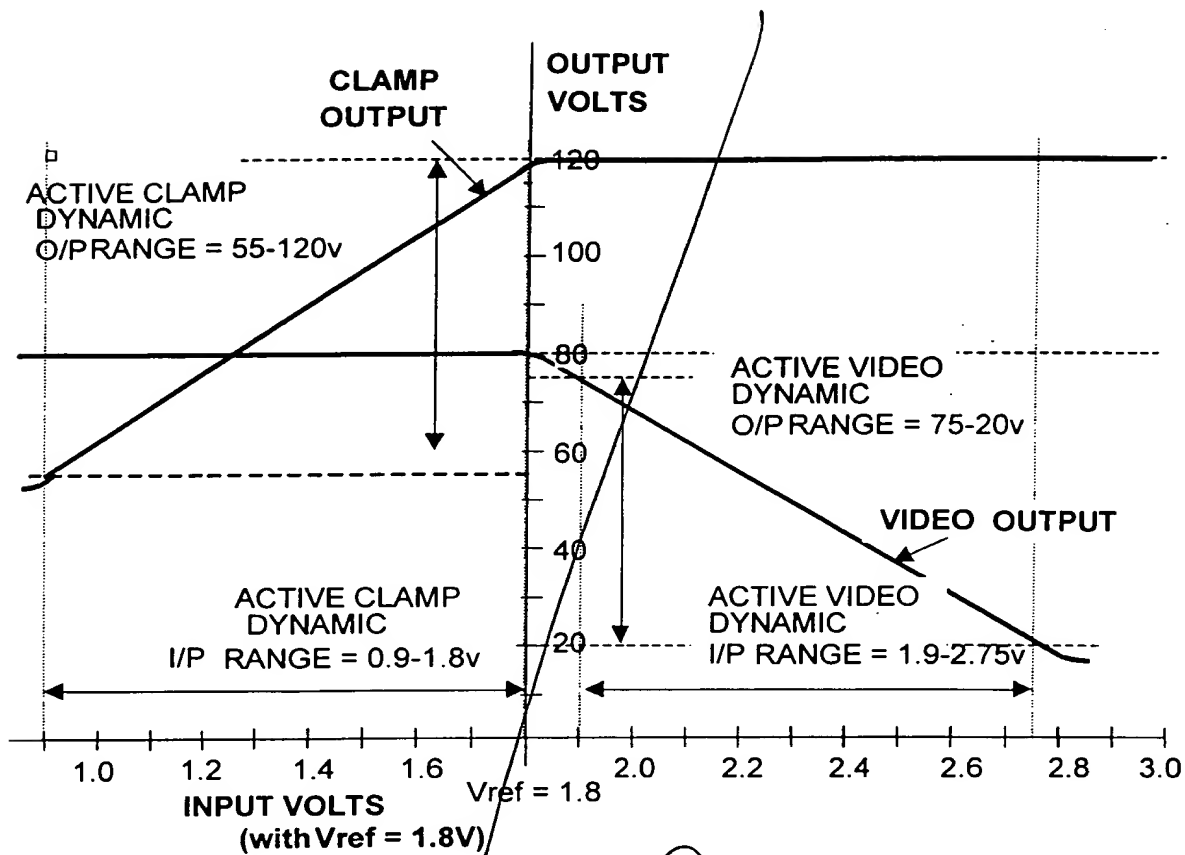


Figure 4: DC I/O Transfer Characteristic for Driver and Clamp Amplifiers  
(Test Conditions:  $V_{ref} = 1.8v$ ,  $V_{cc1} = 80v$ ,  $V_{cc2} = 120v$ ,  $V_{bb} = 12v$ )

Figure 5 shows the operation of the G1 blanking output in combination with the 120V boost operation during start up.

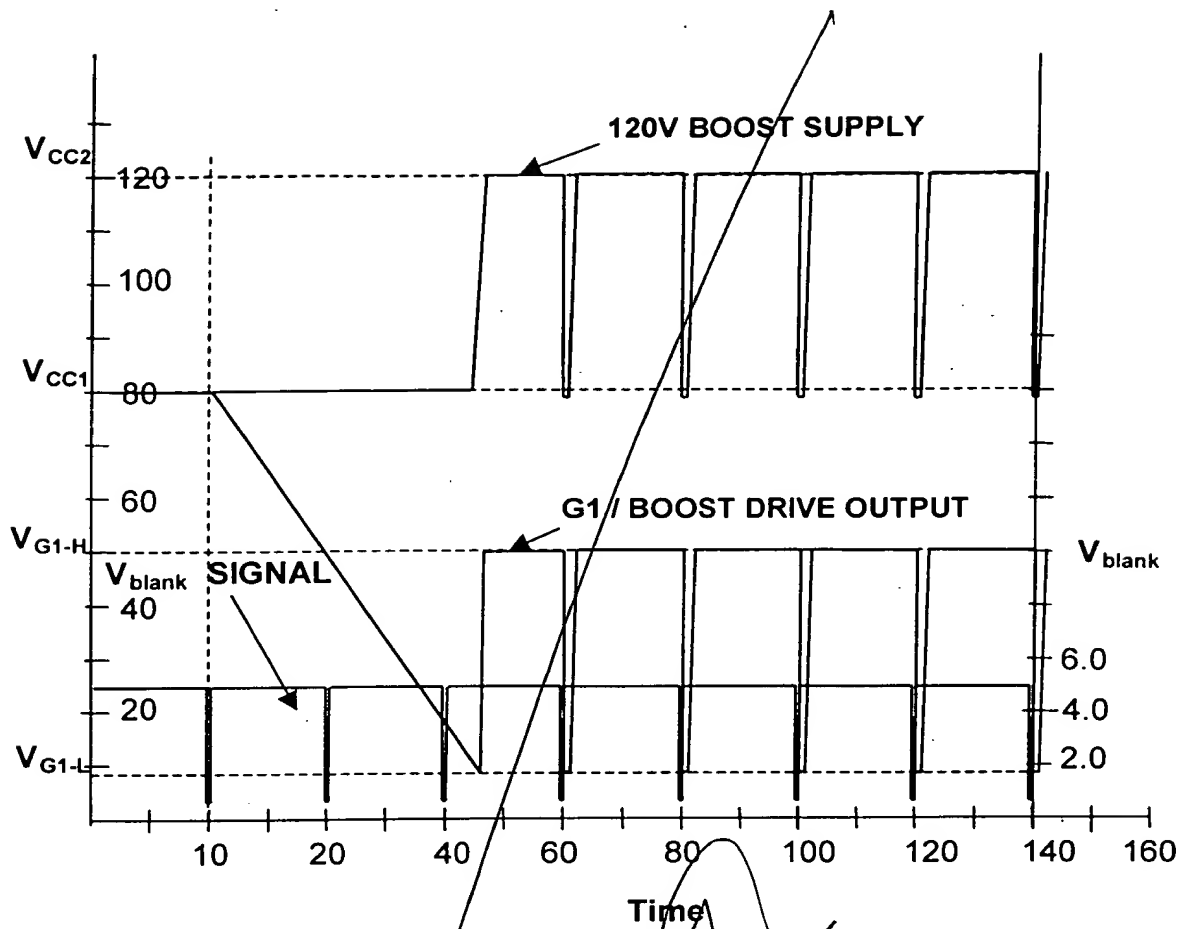


Figure 5: 120v BOOST SUPPLY / G1 BLANKING PULSE OUTPUT AT START UP, SHOWING INITIAL CURRENT LIMITED CHARGE UP

**Limits of Absolute Maximum Ratings (Notes 1 & 3)**

The following parameters will be specified in the data sheet; the specification limits of the device should be within the range specified below:

80v Voltage, $V_{CC1}$	Equal to or better than +90 V
120v Supply $V_{CC2}$	Equal to or better than +130 V
Bias Voltage, $V_{BB}$	Equal to or better than +16 V
Input Voltage, $V_{IN}$	Equal to or better than 0 V to 6 V
Input Reference Voltage, $V_{REF}$	Equal to or better than 0 V to 6 V
VBLANK Input Voltage, $V_{BLANK}$	Equal to or better than 0 V to $V_{BB}$ V
Storage Temperature Range, $T_{STG}$	Equal to or better than -65 °C to +150 °C
Lead Temperature (Soldering, <10 sec.)	Equal to or better than 300 °C
ESD Tolerance, Human Body Model	Equal to or better than 2kV min
ESD Tolerance, Machine Model	Equal to or better than 200V min

Note: the product will be stress tested during manufacturing to 96v at the 80v  $V_{CC1}$  supply input.  
This will stress the  $V_{CC2}$  input to 136v

**Limits of Operating Ranges (Note 2)**

$V_{CC1}$	Equal to or better than +60 V to + 85V
$V_{CC2}$	Equal to or better than $V_{CC1}$ to + 125V
$V_{BB}$	Equal to or better than +8 V to +15 V
$V_{IN}$	Equal to or better than +1 V to +3 V
$V_{REF}$	Equal to or better than +1 V to +3 V
VBLANK Input Voltage, $V_{BLANK}$	Equal to or better than 0 V to 5.5 V
$V_{out}$	Equal to or better than +15 to +75 V
$V_{clamp}$	Equal to or better than +50 to +120 V
$T_{jmax}$	Equal to or better than +150C

**DESIGN FOR ROBUSTNESS:**

The ACDC driver shall be internally laid out to enable the use of series peaking capacitors, and all outputs will use the same size ESD diodes as the 2405C. Any unused devices will be connected with metal in such a manner as to prevent parasitic SCR effects.



**AC DRIVER Electrical Characteristic Targets and Limits** (See Figure 6 for Test Circuit)

Unless otherwise noted:  $V_{CC} = +80\text{ V}$ ,  $V_{BB} = +12\text{ V}$ ,  $V_{IN} = 2.3\text{ VDC}$ ,  $C_L = 8\text{ pF}$ , Output = 40 Vpp at 1 MHz,  $T_C = 50\text{ }^{\circ}\text{C}$ . Vref = 1.80v SW1 open

HEATSINK MUST BE GROUNDED VIA LOW HF IMPEDANCE

The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.

Note: NA means not applicable

0 is a target value means that the ideal value is as low as possible.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
$I_{CC1MAX}$	Maximum Supply Current	All 3 Channels, No Output Load	NA	45		mA
$I_{BBMAX}$	Maximum Bias Current	All three channels	NA	0	60	mA
$V_{OUTTYP}$	Typical DC Output Voltage	No AC Input Signal	48	50	52	V <sub>DC</sub>
$\Delta V_{OUTTYP}$	Variation in DC Output Voltage about typical	No AC Input Signal	NA	0	+/-3v	V <sub>DC</sub>
$A_{vtyp}$	Typical DC Voltage Gain	No AC Input Signal	-62	-65	-68	
$\Delta A_{vtyp}$	Variation of DC Voltage Gain about typical	No AC Input Signal	NA	0	+/-5	
$\Delta A_{vgmtyp}$	Typical Gain Matching between channels	Note 4 / No AC Input Signal	NA	0	1.0	dB
$LE_{typ}$	Typical Linearity Error	Notes 4, 5, No AC Input Signal	NA	0	8	%
$t_{rtyp}$	Typical Rise Time	10% to 90%	5.2	5.5	5.7	nS
$\Delta t_r$	Variation in rise time about typical		NA	0	+/-25	%
$\Delta t_{rch-ch}$	Channel to Channel rise time matching	Note 7	NA	0	+/-15	%
$t_{ftyp}$	Typical Fall Time	90% to 10%	5.2	5.5	5.7	nS
$\Delta t_f$	Variation in fall time about typical		NA	0	+/-25	%
$\Delta t_{fch-ch}$	Channel to Channel fall time matching	Note 8	NA	0	+/-15	%
OS	Typical Overshoot	Rising Edge Falling Edge	NA	0 0	8 2	%
OS <sub>max</sub>	Maximum Overshoot	Rising Edge Falling Edge	NA	-0 0	10 6	%
dt/dT	Variation in response time with temperature	Note 9	NA	0	+/-0.14	%/C

$dt/dC_l$	Variation in response time with load capacitance	Note 10	NA	0	+/-2	%/pf
$dV_{out}/dV_{ref}$	Variation in output with changes in $V_{ref}$	For $1.6V < V_{ref} < 2.0V$	-5	0	5	V/V
$dV_{out}/dV_{bb}$	Variation in output with changes in $V_{bb}$		-0.5	0	0.5	V/V
$dV_{out}/dV_{cc1}$	Variation in output with changes in $V_{cc1}$		-1	0	1	V/V
$dV_{out}/dV_{cc2}$	Variation in output with changes in $V_{cc2}$		-1	0	1	V/V
	CRT Arc Tolerance	Note 11, Tested in Engineering Arc	25	NA	NA	Arcs/Cathode
	Thermal Smear	Tested in Monitor with NSC Neck Board and ACDC Preamp	NA	0	None Visible	
	Overvoltage Stress	$V_{CC} = 96V, V_{BB} = 16V, V_{IN} = V_{ref}$ to 4V, one cycle $V_{CC} = 80V, V_{BB} = 12V, V_{IN} = V_{ref}$ to 4V, 1000 cycles	No damage No damage	NA	NA	
$R_{dd}$	Die Differentiator Resistance	Built input resistance between input and $V_{ref}$	9	10	11	kohm

**Note 1:** Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

**Note 2:** Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

**Note 3:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 4:** Calculated value from Voltage Gain test on each channel.

**Note 5:** Linearity Error is the variation in dc gain from  $V_{in}=2.0$  volts to  $V_{in}=2.6$  volts.

**Note 6:** Input from signal generator:  $t_r, t_f < 1$  nS.

**Note 7:**  $\Delta t_{rch-ch} = 200 \cdot (t_{rch-a} - t_{rch-b}) / (t_{rch-a} + t_{rch-b}) \%$

Where:

- channel a and channel b are any two channels within the same device
- $t_{rch-a}$  and  $t_{rch-b}$  refers to the rise time of channel a and channel b.

**Note 8:**  $\Delta t_{fch-ch} = 200 \cdot (t_{fch-a} - t_{fch-b}) / (t_{fch-a} + t_{fch-b}) \%$

Where:

- channel a and channel b are any two channels within the same device
- $t_{fch-a}$  and  $t_{fch-b}$  refers to the fall time of channel a and channel b.

**Note 9:**  $dt/dT = 200 \cdot (t_{100C} - t_{40C}) / ((t_{100C} + t_{40C}) \cdot 60) \% / C$

Where:

- $t_{40C}$  is the rise or fall time at 40C
- $t_{100C}$  is the rise or fall time at 100C case temperature.

**Note 10:**  $dt/dC_l = 200 \cdot (t_{20pf} - t_{8pf}) / ((t_{20pf} + t_{8pf}) \cdot 12) \% / pf$

Where:

- $t_{20pf}$  is the rise or fall time with 20pf load
- $t_{8pf}$  is the rise or fall time with 8pf load.

## OTHER PRODUCT REQUIREMENTS

The device should have a class AB output stage, and should exhibit no small signal cross-over distortion without the need for any external resistive load. The small signal rise and fall times at 1vp-p should be within +/- 20% of the large signal values.

Any change in bandwidth with output signal magnitude should be smooth and continuous, with no rapid changes in gain.

- ## DRIVER Test Circuit

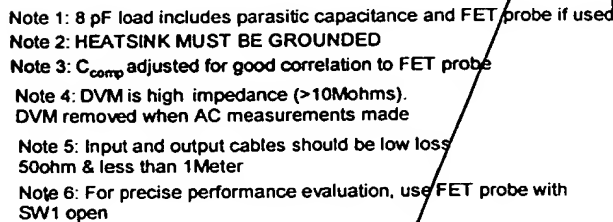


Figure 6 shows a typical test circuit for evaluation of the ACDC DRIVER. For precise evaluation, a calibrated FET probe should be used. This circuit is also allows testing of the ACDC DRIVER in a 50 ohm environment without the use of an expensive FET probe. The 4950 ohm resistor at the output forms a 200:1 voltage divider when connected to a 50 ohm load. Ccomp must be adjusted for equivalent performance to the FET probe, though performance may be affected by the effect of the load of the 5k.

**DC CLAMP Electrical Characteristic Targets and Limits** (See Figure 7 for Test Circuit)

Unless otherwise noted:  $V_{CC1} = +80\text{ V}$ ,  $V_{CC2} = +120\text{ V}$ ,  $V_{BB} = +12\text{ V}$ ,  $V_{IN} = 1.8\text{ VDC}$ ,  $T_C = 50^\circ\text{C}$ ,  $V_{ref} = 1.80\text{ v}$ , SW1 open.

HEATSINK MUST BE GROUNDED VIA LOW HF IMPEDANCE

The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.

Note: NA means not applicable

0 is a target value means that the ideal value is as low as possible.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
$I_{CC2MIN}$	Maximum DC Supply Current at $V_{outmin}$	Per Channel, No AC input signal, $V_{in}=1.25\text{ v}$	NA	0	1.2	mA
$I_{CC2MAX}$	Maximum DC Supply Current at $V_{outmax}$	Per Channel, No AC input signal, $V_{in}=1.75\text{ v}$	NA	0	0.1	mA
$V_{OUTTYP}$	Typical DC Output Voltage	No AC Input Signal, $V_{in}=1.5\text{ V}$	88	90	92	$V_{DC}$
$\Delta V_{OUTTYP}$	Variation in DC Output Voltage about typical	No AC Input Signal, $V_{in}=1.5\text{ v}$	NA	0	$\pm 3\text{ v}$	$V_{DC}$
$A_{vtyp}$	Typical DC Voltage Gain	No AC Input Signal	72	75	78	
$\Delta A_{vtyp}$	Variation of DC Voltage Gain about typical	No AC Input Signal	NA	0	$\pm 4$	
$\Delta A_{vgmtyp}$	Typical Gain Matching between channels	No AC Input Signal	NA	0	1.0	dB
$LE_{typ}$	Typical Linearity Error	No AC Input Signal, See Note 4	NA	0	8	%
$t_{fyp}$	Typical Fall Time	90% to 10%	0	0	500	nS
$OS_{max}$	Maximum Overshoot	Falling Edge	0	0	None	%
$R_{out}$	Typical output resistance	$V_{in} = 1.5\text{ v}$ , Clamp active See Note 5 and test circuit	0	0	200	ohms
$dV_{out} / dV_{bb}$	Variation in output with changes in $V_{bb}$		-0.5	0	0.5	V/V
$dV_{out} / dV_{ref}$	Variation in output with changes in $V_{ref}$	For $1.6\text{ v} < V_{ref} < 2.0\text{ v}$	-5	0	5	V/V
$dV_{out} / dV_{cc}$	Variation in output with changes in $V_{cc}$		-1	0	1	V/V
$dV_{out} / dV_{cc2}$	Variation in output with changes in $V_{cc2}$		-1	0	1	V/V
$dV_{out}/dT$	Variation in output with temperature	At any output voltage setting, compared to $V_{in}=1.5\text{ v}$ at $25^\circ\text{C}$ $T_{case} = 15^\circ\text{C}-100^\circ\text{C}$	0	0	$\pm 0.25$	V

	CRT Arc Tolerance	Note 11, Tested in Engineering Arc	25	NA	NA	Arcs/ Cathode
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**Note 1:** Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

**Note 2:** Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

**Note 3:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 4:** Linearity Error is the variation in dc gain from  $V_{in}=1.3$  volts to  $V_{in}=1.7$  volts.

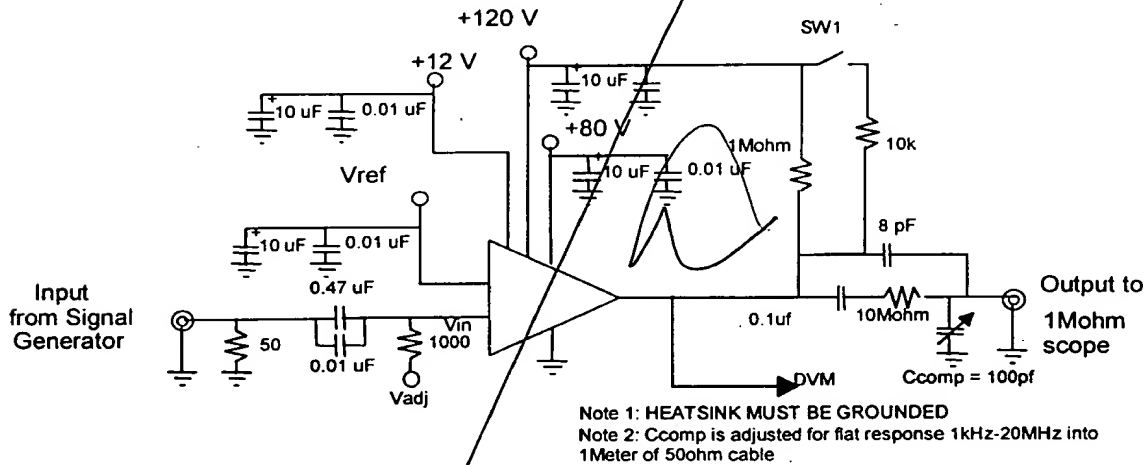
**Note 5:** Calculated value when SW1 is closed:

$$R_{out} = \frac{(V_{open} - V_{closed}) * 10K\Omega}{V_{closed}}$$

Where:

- $V_{open}$  is the output voltage when SW1 is open
- $V_{closed}$  is the output voltage when SW1 is closed

### Clamp Amplifier Test Circuit



**FIGURE 7. Test Circuit (One Channel)**

Figure 7 shows a typical test circuit for evaluation of the ACDC clamp amplifier. A high impedance DVM (>10Mohm) should be used for DC measurements at the outputs. Vadj is adjusted to the value  $V_{in}$  as specified in the specification table.

Spread means variation of parameter in production with tolerance

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$\Delta V_{G1pp}/dT$	Variation in 120V boost supply with temperature	At any output voltage setting, compared to 25C Tcase =15C-100C	0	0	+/-0.5	V
$T_{G1typ}$	Typical Rise Time	10% to 90%, see Note 8	0	0	20	uS
$T_{G1fyp}$	Typical Fall Time	10% to 90%, see Note 8	0	0	5	uS
$dV_{120BOOST}/dV_{bb}$	Variation in 120v boost supply with changes in $V_{bb}$		0	0	+/-1	V/V
$dV_{120BOOST}/dV_{cc}$	Variation in 120v boost supply with changes in $V_{cc}$		0	0	+/-1	V/V
	CRT Arc Tolerance	Note 11, Tested in Engineering Arc	25	NA	NA	Arcs/ Cathode

**Note 1:** Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

**Note 2:** Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

**Note 3:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 4:** Calculated value from Voltage Gain test on each channel.

**Note 5:** Calculated value of Vref output resistance when SW2 is closed:

$$R_{out} = \frac{(V_{closed} - V_{open}) * 10k\Omega}{\{2.8 + V_{open} - (2 * V_{closed})\}}$$

Where:

- $V_{open}$  is the Vref output voltage when SW2 is open
- $V_{closed}$  is the Vref output voltage when SW2 is closed

**Note 6:** Calculated variation in video output voltage when SW2 is closed:

$$dV_{r,g,bout}/dI_{ref} = \frac{(V_{r,g,b open} - V_{r,g,b closed}) * 40k\Omega}{2.8 - V_{ref}}$$

Where:

- $V_{r,g,b open}$  is any video output voltage when SW2 is open
- $V_{r,g,b closed}$  is any video output voltage when SW2 is closed

**Note 7:** Calculated value of 120V boost output resistance when SW1 is closed:

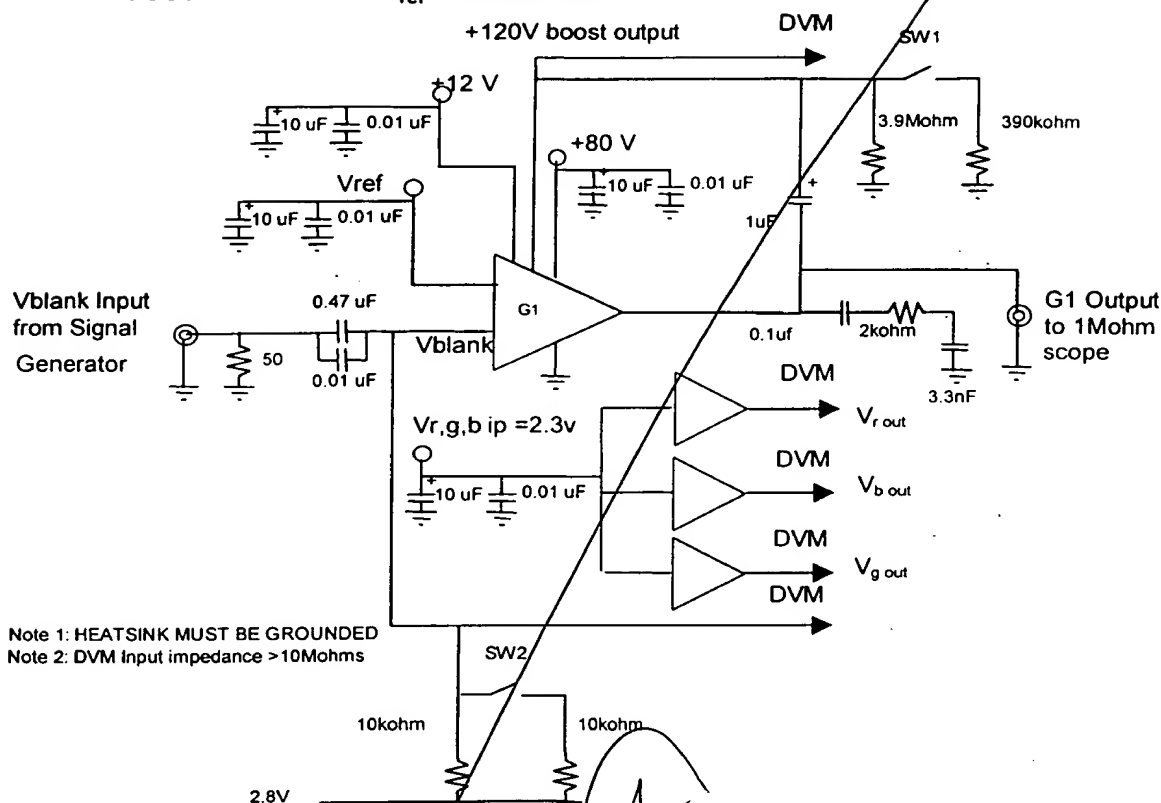
$$R_{out} = \frac{(V_{open} - V_{closed}) * 390k\Omega}{V_{closed}}$$

Where:

- $V_{open}$  is the 120v boost output voltage when SW1 is open
- $V_{closed}$  is the 120v boost output voltage when SW1 is closed

**Note 8:** Input from signal generator: 2vp-p pulse:  $t_{high} = 300\mu s$ ,  $t_{low} = 10ms$ , 2v p-p. rise/fall time <0.1us

### 120V Boost / G1 Drive $N_{ref}$ Test Circuit



**FIGURE 8. 120V Boost /G1 /  $V_{ref}$  Drive Test Circuit**

**REVISION HISTORY:**

**V0.14 Sept 98:**

Figure 6 changed to show FET probe as preferred AC measurement method  
Polarity of Vblank pulse changed to negative going. Table and Figures 5 & 8  
changed to reflect these changes.

V0.15 10/13/98: Figure 2 changed to include pin out of device. Added feature list on page 2.

V0.17 12/24/98: Spec changed to reflect removing Vref. Gain of clamp circuit reduced to 72.



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# ~~APPENDIX B~~

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DO NOT SEE 950



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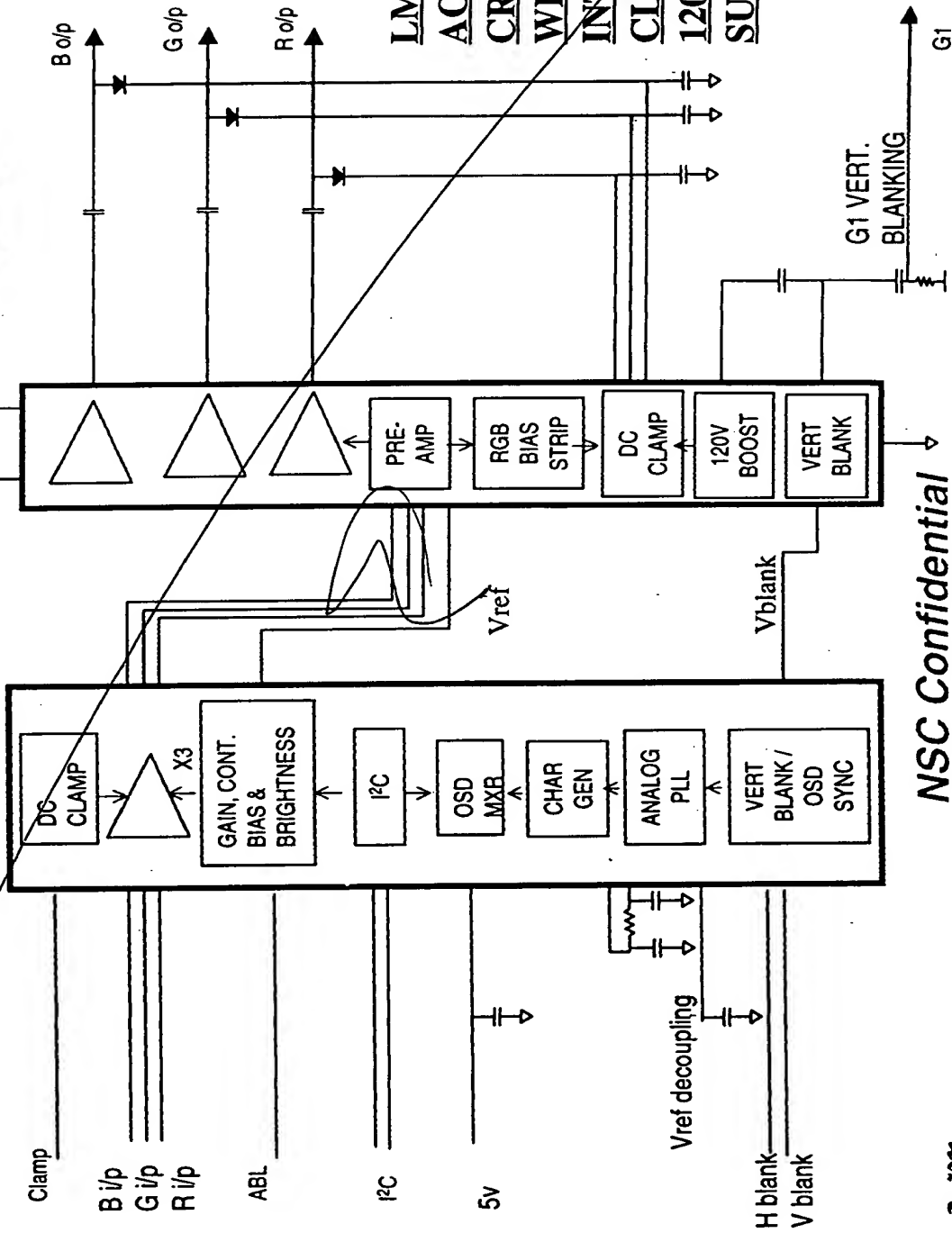
AC<sub>2</sub>DC

# NEW AC<sub>2</sub>DC SYSTEM

ARC PROTECTION,  
ESD, INPUT  
TERMINATION  
ETC NOT SHOWN

**LM1253: CMOS I<sup>2</sup>C**  
**OSD-GEN + PRE-AMP**

**STRICTLY  
CONFIDENTIAL**



NSC Confidential

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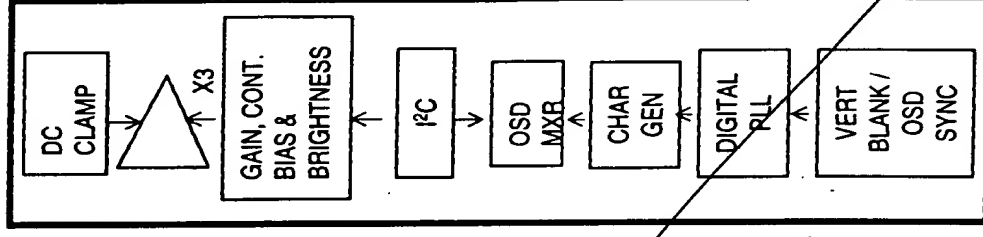


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AC2DC

# LM1253: I<sup>2</sup>C OSD GENERATOR + PRE-AMP

- 0.35u 5v CMOS OSD/PRE-AMP - LM1253
  - ◆ state of the art process
  - ◆ many future integration possibilities (eg uC, USB, DDC etc)
  - ◆ first device in new family of OSD-Preamps
- Single low cost package (28pin DIL)
- I<sup>2</sup>C controlled OSD and all pre-amp functions
- Videoplex driver interface video signal
  - ◆ OSD
  - ◆ DC bias and brightness
  - ◆ H blank
  - ◆ Video signal
- Single 5v, 0.25mA supply
  - ◆ low power standby mode
- Easy interface to Hflyback, Vflyback, ABL
  - ◆ internal clamping - only one external resistor for flyback interface
  - ◆ vertical blanking duration controlled by digital counter
- High input impedance - low smear
- Bi-directional output drive - good symmetry



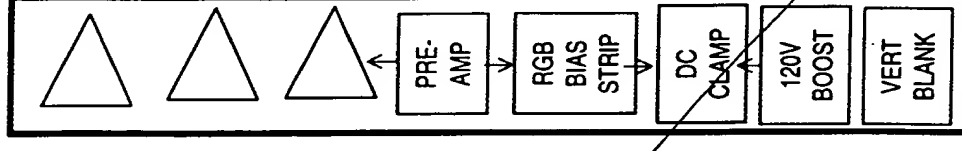


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AC2DC

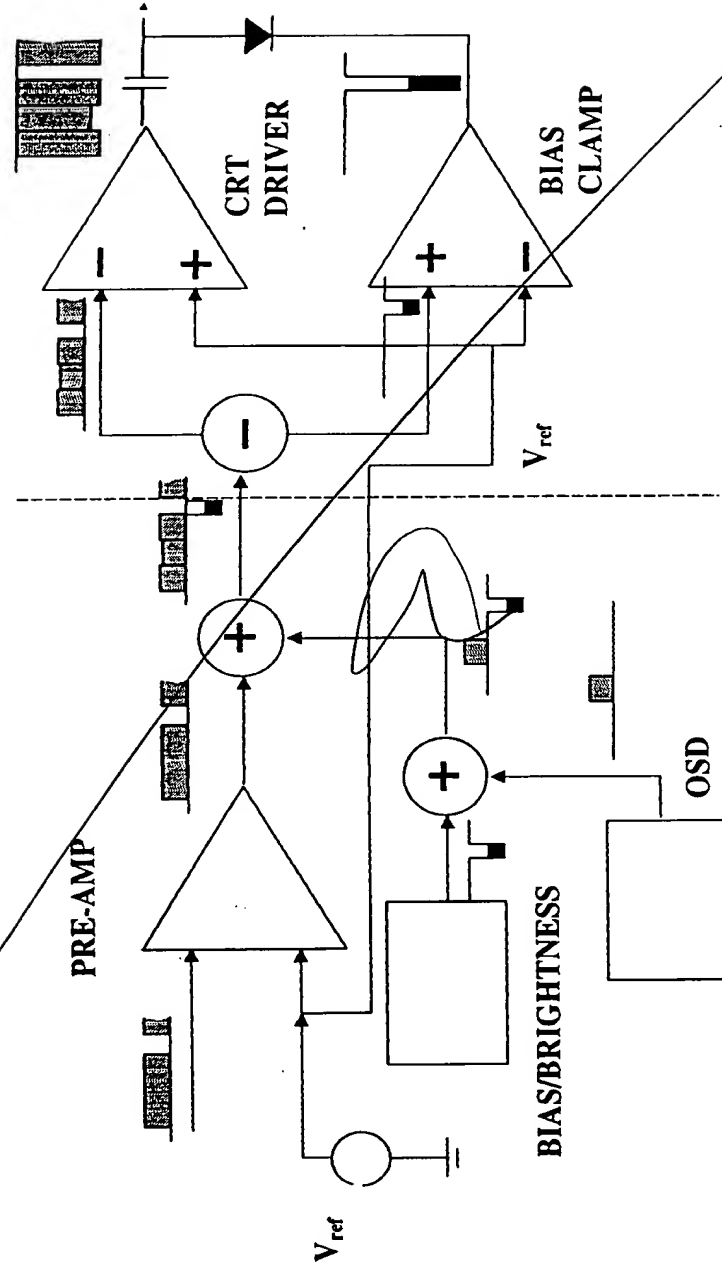
## INTEGRATED AC DRIVER/CLAMP

- Similar to today's open loop AC driver designs
  - ◆ uses existing NSC low power technology (eg LM2415 etc)
  - ◆ 75-85v Vcc for lowest AC power
  - ◆ higher gain (50X)
  - ◆ differential input to give good DC stability at higher gain
- DC bias clamp function
  - ◆ ultra low power operation
  - ◆ >60V DC adjustment range
  - ◆ allows brightness and bias functions
- G1 vertical blank generator / 120v capacitor boost circuit
  - ◆ 40v p-p vertical blanking pulse
  - ◆ boost circuit for bias clamp circuit



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# AC<sub>2</sub>DC SYSTEM BLOCK DIAGRAM



PRE-AMP

DRIVER/CLAMP

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AC2DC

# ACDC VALUE PROPOSITION v LM1279

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						\$1.20	\$1.35	\$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			\$0.20	\$0.35	\$0.50
PWM FILTERS			8	8			\$0.04	\$0.08	\$0.10
PREAMP	LM1279						\$0.45	\$0.55	\$0.65
256char PWM OSD GEN	MYSONX MQTO						\$0.85	\$1.10	\$1.45
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)				2	1	3	\$0.10	\$0.12	\$0.15
PCB MATERIAL SAVINGS						20-30%	\$0.02	\$0.08	\$0.15
SMALLER EMI SHIELD						20-30%	\$0.02	\$0.08	\$0.15
G1 VERT BLANKING		1	4	1			\$0.03	\$0.05	\$0.07
G1 BRIGHTNESS CONTROL		1	4	1			\$0.03	\$0.05	\$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		\$0.03	\$0.06	\$0.08
H FLYBACK LEVEL CLAMPS				1	2		\$0.01	\$0.02	\$0.03
PRE-AMP DC DECOUPLING CAPS				6			\$0.04	\$0.06	\$0.08
TOTAL SYSTEM VALUE							\$3.02	\$3.95	\$4.98

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**ACDC VALUE PROPOSITION v TDA4886**

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						\$1.20	\$1.35	\$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			\$0.20	\$0.35	\$0.50
PWM FILTERS			4	4			\$0.02	\$0.04	\$0.05
I2C PREAMP	TDA4886						\$0.70	\$0.80	\$0.90
256char OSD GEN	MYSON / MOTO						\$0.70	\$0.80	\$1.00
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)				2	1	3	\$0.10	\$0.12	\$0.15
PCB MATERIAL SAVINGS						20-30%	\$0.02	\$0.08	\$0.15
SMALLER EMI SHIELD						20-30%	\$0.02	\$0.08	\$0.15
G1 VERT BLANKING		1	4	1			\$0.03	\$0.05	\$0.07
G1 BRIGHTNESS CONTROL		1	4	1			\$0.03	\$0.05	\$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		\$0.03	\$0.06	\$0.08
H FLYBACK LEVEL CLAMPS				1	2		\$0.01	\$0.02	\$0.03
PRE-AMP DC DECOUPLING CAPS				6			\$0.04	\$0.06	\$0.08
TOTAL SYSTEM VALUE							\$3.10	\$3.86	\$4.73

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AC2DC

# ACDC VALUE PROPOSITION v LM1279

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						\$1.20	\$1.35	\$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			\$0.20	\$0.35	\$0.50
PWM FILTERS			8	8			\$0.04	\$0.08	\$0.10
PREAMP	LM1279						\$0.45	\$0.55	\$0.65
256char PWM OSD GEN	MYSON / MOTO						\$0.85	\$1.10	\$1.45
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)			2	1	3		\$0.10	\$0.12	\$0.15
PCB MATERIAL SAVINGS					20-30%		\$0.02	\$0.08	\$0.15
SMALLER EMI SHIELD					20-30%		\$0.02	\$0.08	\$0.15
G1 VERT BLANKING		1	4	1			\$0.03	\$0.05	\$0.07
G1 BRIGHTNESS CONTROL		1	4	1			\$0.03	\$0.05	\$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		\$0.03	\$0.06	\$0.08
H FLYBACK LEVEL CLAMPS				1	2		\$0.01	\$0.02	\$0.03
PRE-AMP DC DECOUPLING CAPS				6			\$0.04	\$0.06	\$0.08
TOTAL SYSTEM VALUE							\$3.02	\$3.95	\$4.98

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# ACDC VALUE PROPOSITION v TDA4886

FUNCTION	IC	TRANS	R'S	C'S	D'S	OTHER	LOW	MID	HIGH
AC DRIVER	LM2435						\$1.20	\$1.35	\$1.50
DIGITALLY CONTROLLED AC CLAMP		6	9	3			\$0.20	\$0.35	\$0.50
PWM FILTERS			4	4			\$0.02	\$0.04	\$0.05
I2C PREAMP	TDA4886						\$0.70	\$0.80	\$0.90
256char OSD GEN	MYSON / MOTO						\$0.70	\$0.80	\$1.00
120V SUPPLY (WINDING+DIODE+CAP+WIRE+ FILTER BEAD)			2	1	3		\$0.10	\$0.12	\$0.15
PCB MATERIAL SAVINGS						20-30%	\$0.02	\$0.08	\$0.15
SMALLER EMI SHIELD						20-30%	\$0.02	\$0.08	\$0.15
G1 VERT BLANKING		1	4	1			\$0.03	\$0.05	\$0.07
G1 BRIGHTNESS CONTROL		1	4	1			\$0.03	\$0.05	\$0.07
VERT FLYBACK PULSE CLAMP & STRETCH		1	4	1	2		\$0.03	\$0.06	\$0.08
H FLYBACK LEVEL CLAMPS				1	2		\$0.01	\$0.02	\$0.03
PRE-AMP DC DECOUPLING CAPS				6			\$0.04	\$0.06	\$0.08
TOTAL SYSTEM VALUE							\$3.10	\$3.86	\$4.73



# LM1253

## OSD GENERATOR AND PRE-AMP

### FAE TRAINING SPECIFICATION

THIS DOCUMENT IS A PRELIMINARY SPECIFICATION FOR THE LM1253 FOR THE PURPOSE OF FAE TRAINING. ALL INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE. THE PIN-OUT FOR THE DEVICE IS NOT FINALIZED.

THIS DOCUMENT IS CONFIDENTIAL AND THE INFORMATION CONTAINED WITHIN SHOULD NOT BE DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR AGREEMENT.

NSC DISPLAYS GROUP

7/2/99

V0.1

AUTHOR: Andy Morrish



**National**  
Semiconductor



Preliminary

Mar, 1999

Information contained herein is  
subject to change without notice.

## **AC-DC OSD GENERATOR AND PRE-AMP OVERVIEW**

### **MONOLITHIC TRIPLE 150MHz I<sup>2</sup>C CRT PREAMP WITH INTEGRATED OSD**

This is a preliminary product specification for the LM1253 pre-amp and OSD generator to be used in the AC<sub>2</sub>DC™ system. The parameters defined in this document specify the design target value for critical performance attributes of the device.

#### **FEATURES:**

150MHz preamplifier with full video signal parametric control  
Channel Gain corrected Brightness and OSD control  
Videoplex™ interface to AC<sub>2</sub>DC™ driver  
OSD mixing with 64 out of 512 color mask programmable selection  
190 two-color ROM based Character Fonts with individual character attribute  
64 four-color ROM based Character Fonts with individual character attribute  
Programmable window size with up to 512 character and line definition codes  
Support for 2 independent Display Windows (size of each window is configurable)  
Programmable start position for each Display Window  
Programmable Resolutions: from 512 to 960 pixels per line in 64 pixel increments  
Programmable Character Height, with automatic height control with mode change  
Programmable blank line spacing between each display character row  
Maximum Pixel clock of 92.2 MHz, maximum line rate 125kHz  
I<sup>2</sup>C compatible interface to system micro-controller  
Programmable color Windows95™ style 'button boxes', shadows, borders  
Programmable period vertical blanking pulse  
Easy interface to H and V flyback pulses for video blanking

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## **1 PREAMPLIFIER**

### **1.1 PRE-AMP GENERAL DESCRIPTION**

The LM1253 pre-amp is an integrated high voltage triple CRT pre-amp and On Screen Display (OSD) generator. The IC is I<sup>2</sup>C controlled, and allows control of all the parameters necessary to setup and adjust the brightness and contrast in the CRT display. In addition, it provides a programmable period vertical blanking pulse which is used to blank the G1.

The LM1253 pre-amp is designed to work in cooperation with AC<sub>2</sub>DC™ drivers, such as the LM2453, and provides a multiplexed video signal (Videoplex™) interface to enable the DC clamp levels of AC coupled signals at the cathode to be varied in order to set up the CRT bias and to allow individual adjustment for brightness.

The OSD has a selectable palette allowing a wide selection of colors. The preset contrast level of the OSD can be controlled by I<sup>2</sup>C to suit different CRT displays. The OSD signal is internally mixed with the video signal, before the gain section, and thus gives excellent white tracking of the OSD with the white color point setting of the video.

The Brightness settings are also mixed into the video signal before the gain matching controls and consequently give excellent white color point tracking with variations in the Brightness control.

An active horizontal blanking signal is added to the video at the output, giving excellent smear performance, and preventing video content dependant DC bias offsets as a result of high frequency over shoot.

The OSD horizontal sync and blanking signal is derived from a positive going flyback pulse. The digital section provides easy interfacing of this signal with the deflection circuits.

The vertical blanking signal is taken from the vertical sync signal, and the blanking duration is programmable. The AC<sub>2</sub>DC™ system is highly integrated and requires a minimal number of external components.

Black level clamping of the signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional black level clamp capacitors.

The outputs are referenced to a DC level produced by the AC<sub>2</sub>DC™ pre-amp, and so provide stable DC operating levels within the system without the need for additional external feedback components.

The IC is packaged in an industry standard wide body 28 lead DIL molded plastic package.

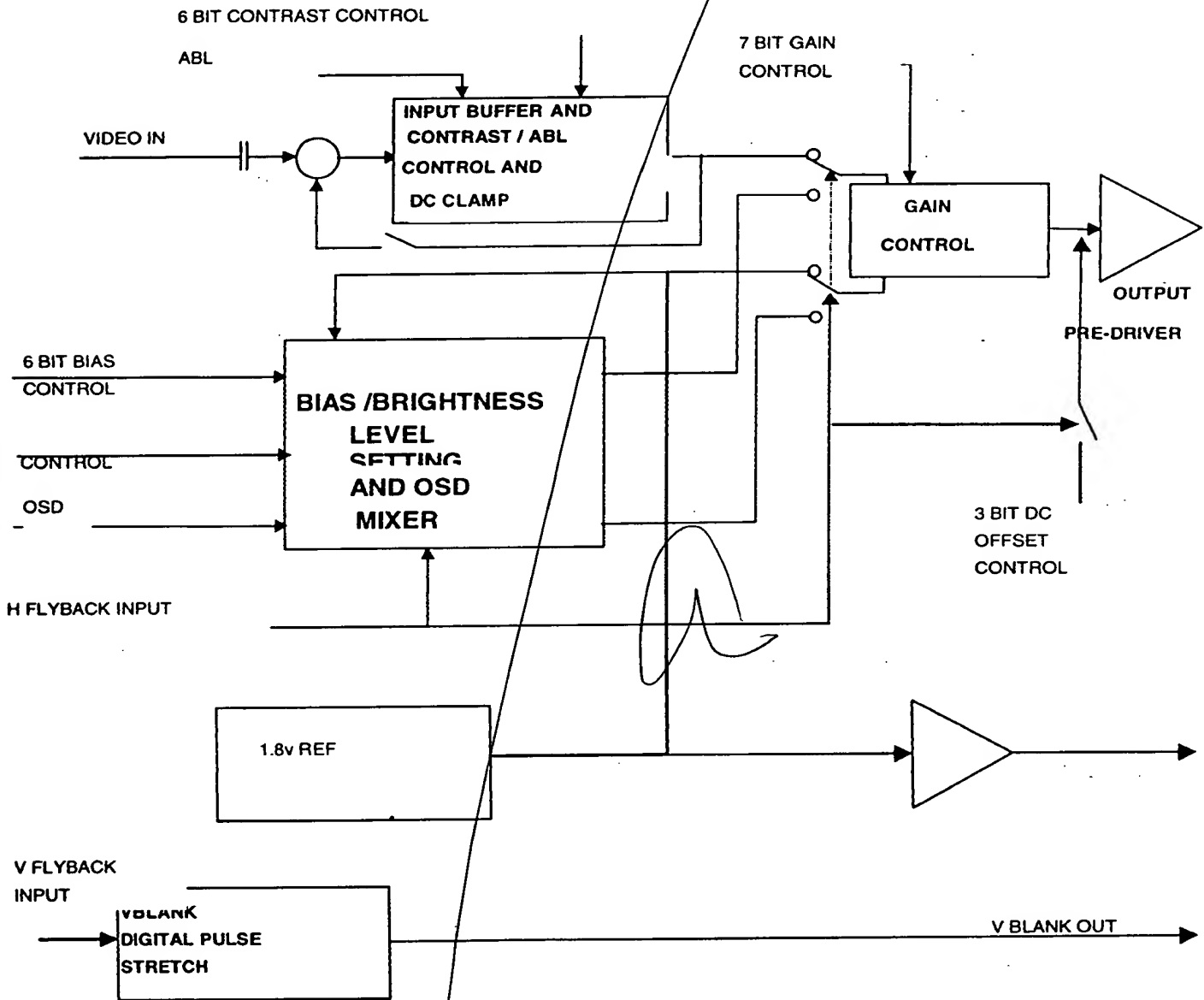
### **1.2 INTENDED APPLICATIONS**

This device is intended for use in applications with the LM2453 AC<sub>2</sub>DC™ driver. This makes the device ideally suited for 1280x1024 at 75Hz. Some customers may be able to obtain useful performance up to 1280x1024 at 85Hz., depending upon the individual customers criteria for how much bandwidth is required for a given application. Target

# LM1253 PREAMP+ OSD GENERATOR: V0

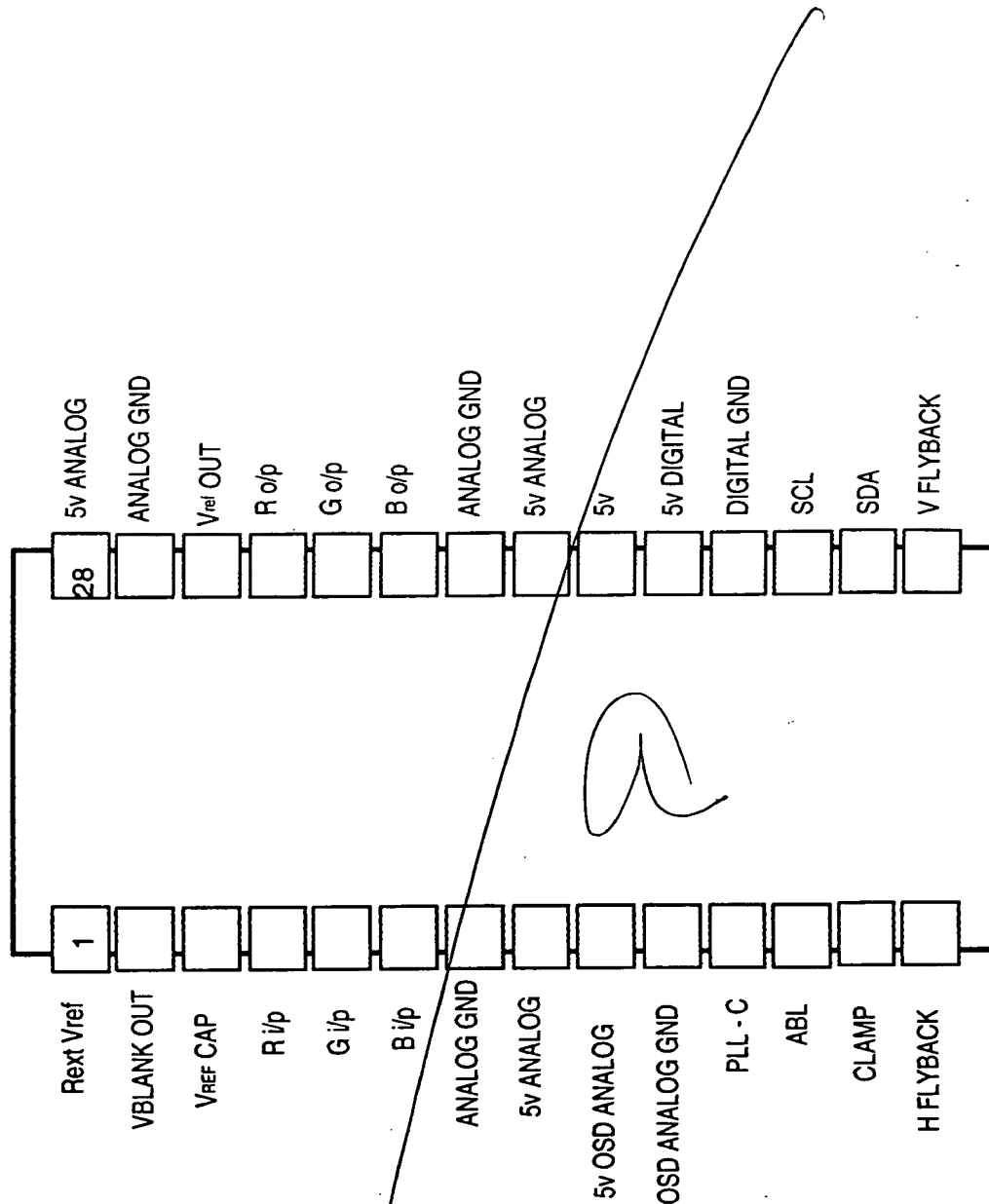
applications running at these speeds are mid range 15" and 17" monitors.

## 1.3 BASIC APPLICATION SCHEMATIC AND CONNECTION DIAGRAMS



**Figure 1 LM1253 PRE-AMP BLOCK DIAGRAM**

LM1253 PREAMP+ OSD GENERATOR: V0.1



**Figure 2 TOP VIEW (FINAL PIN OUT TO BE DETERMINED)**



LM1253 PREAMP + OSD GENERATOR: V0.1

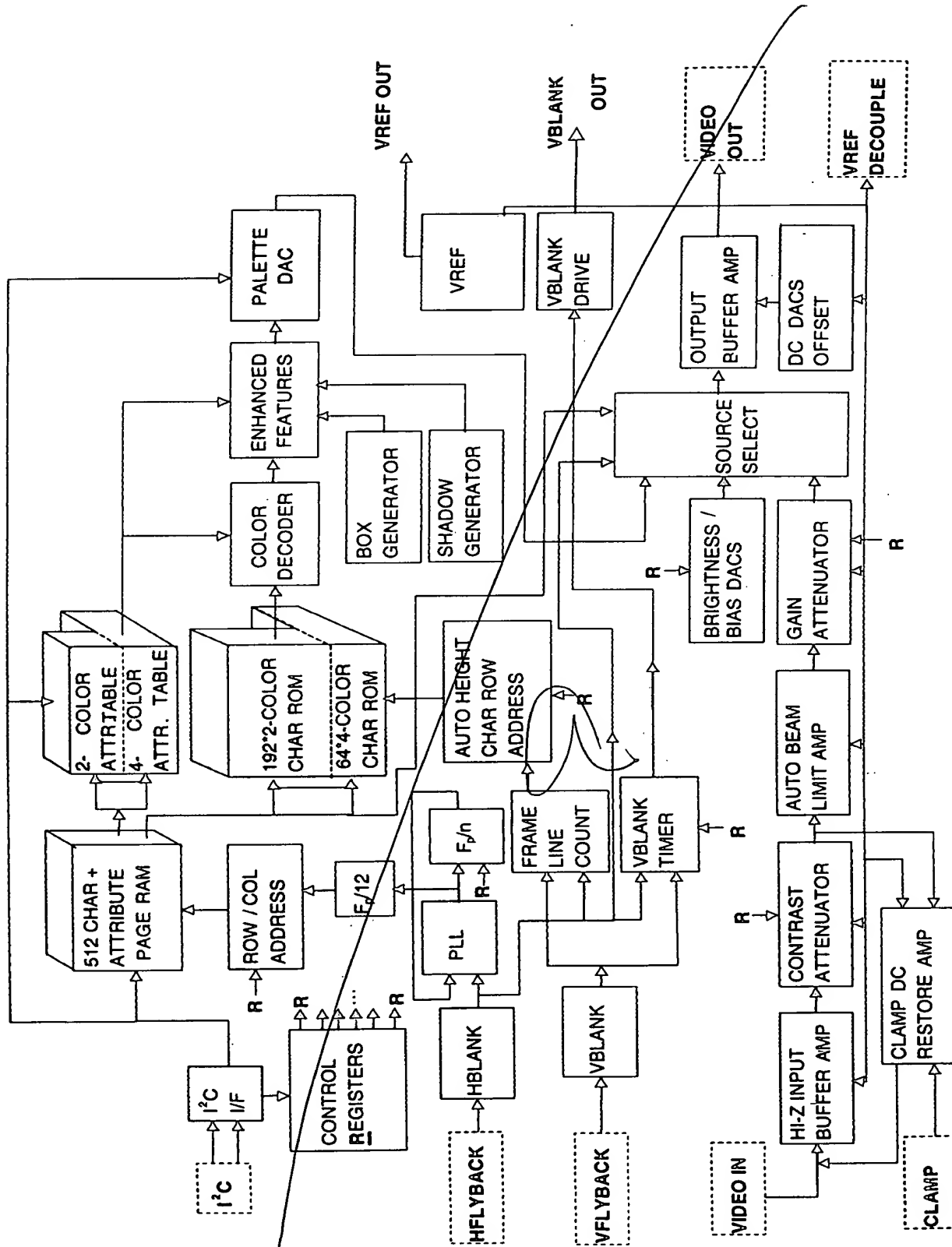


Figure 3 LM1253 BLOCK DIAGRAM (ONE CHANNEL)

LM1253 PREAMP+ OSD GENERATOR: V0.1

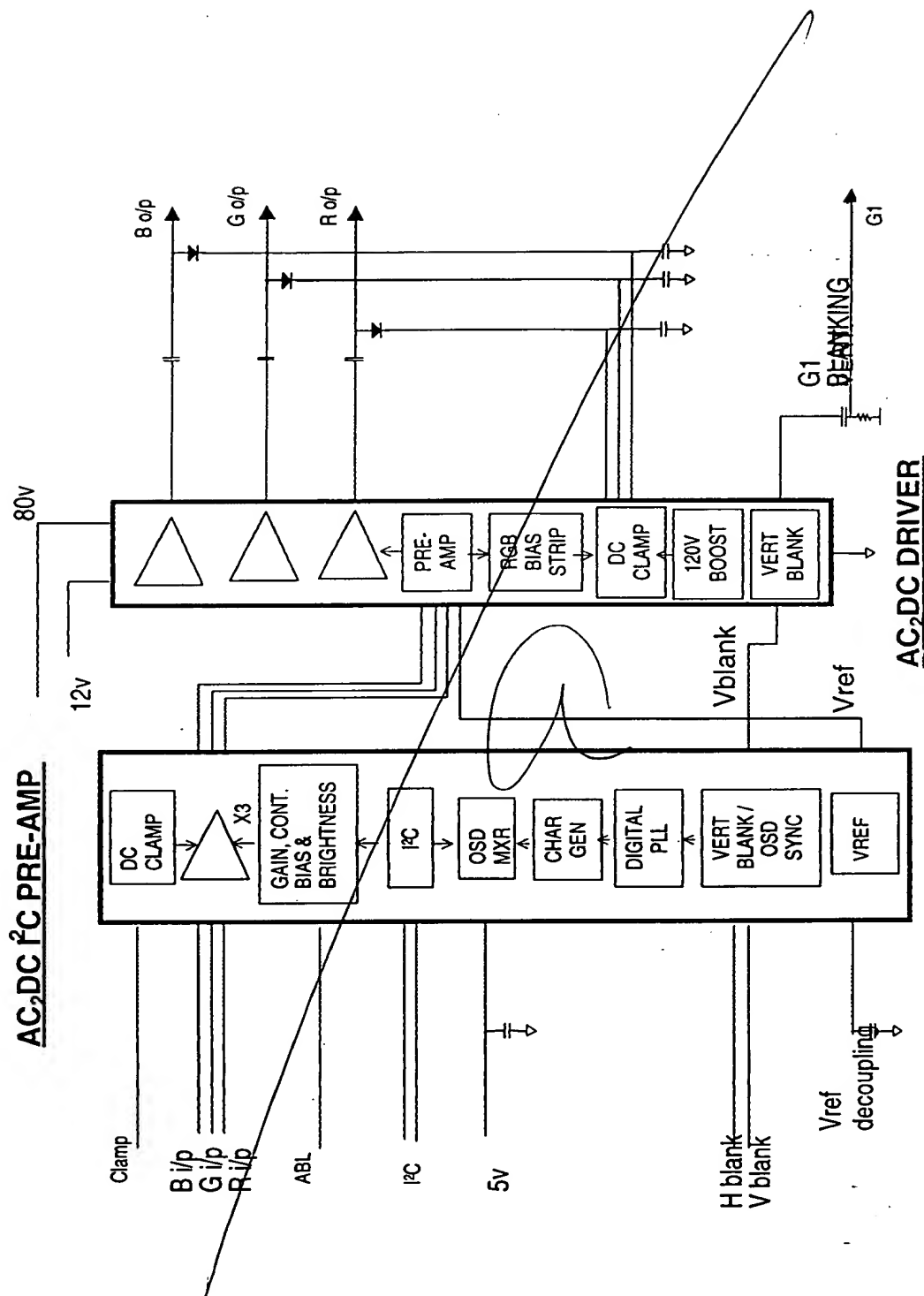
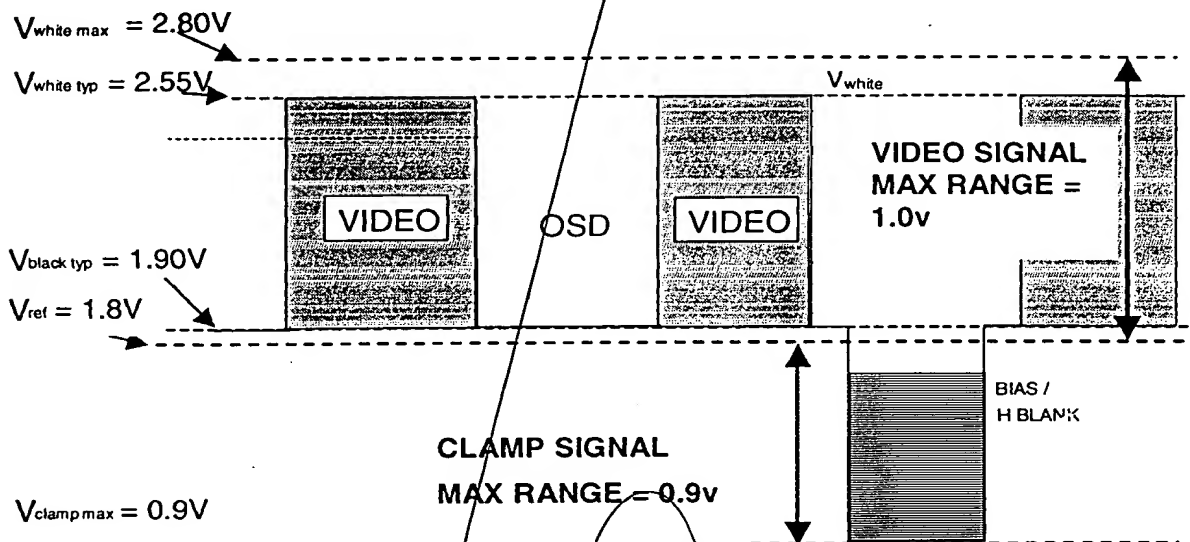


Figure 4 SIMPLIFIED SCHEMATIC DIAGRAM

#### 1.4 SPECIAL FEATURES

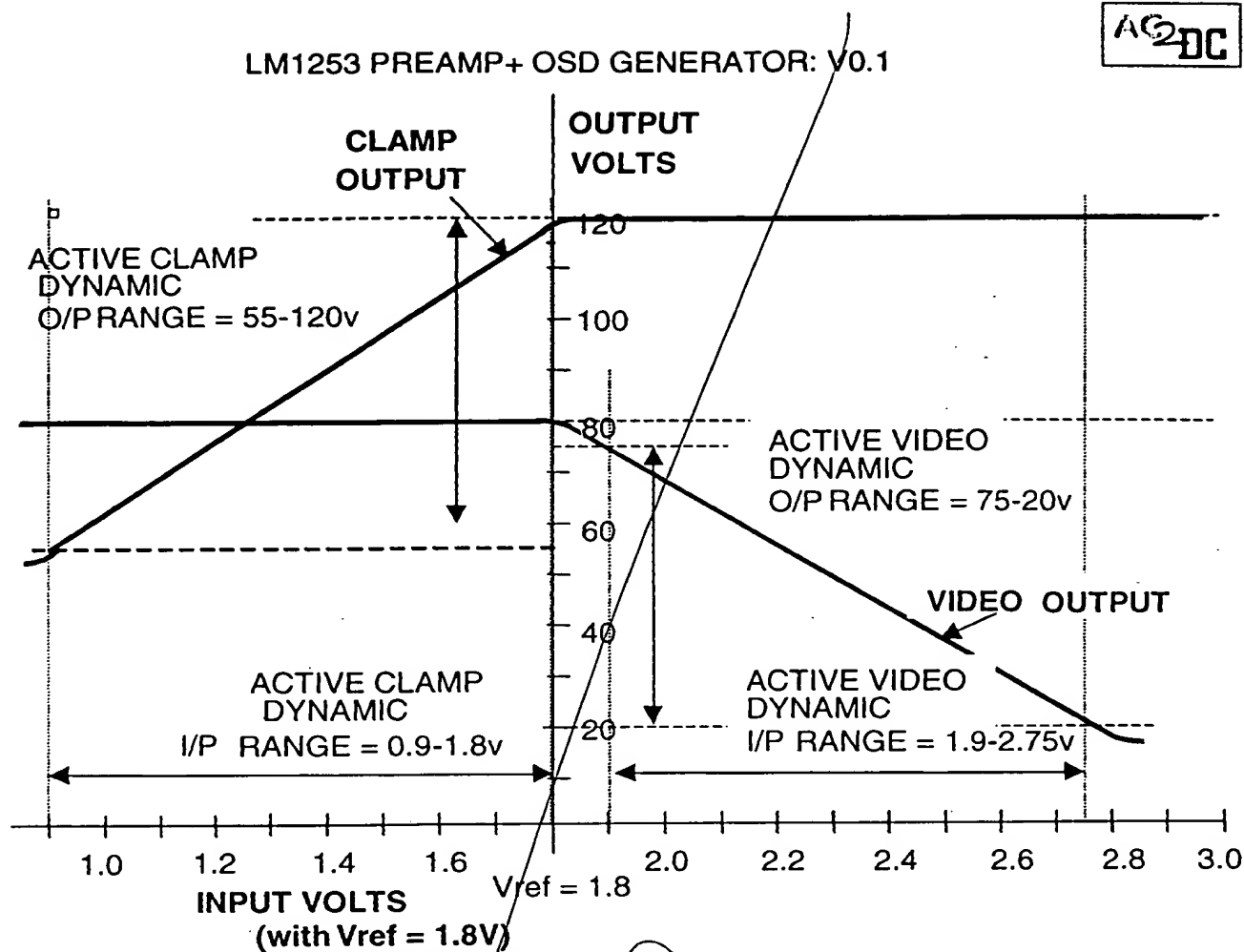
The AC<sub>2</sub>DC™ system using the National Videoplex™ multiplexed video signal to send the video signal and DC clamp level from preamplifier to driver. The basic signal scheme is shown in the figure below.



**Figure 5 AC<sub>2</sub>DC™ SYSTEM VIDEOPLEX™ VIDEO SIGNAL**

The response to the video and clamp amplifiers to the Videoplex™ signal is shown in the figure below.

LM1253 PREAMP+ OSD GENERATOR: V0.1



**Figure 6 DC I/O TRANSFER CHARACTERISTIC FOR DRIVER AND CLAMP AMPLIFIERS**

(Test Conditions:  $V_{ref} = 1.8v$ ,  $V_{cc1} = 80v$ ,  $V_{cc2} = 120v$ ,  $V_{bb} = 12v$ )

### 1.5 ACTIVE VIDEO TRANSFER CHARACTERISTIC

The nominal value of the active signal at the output shall vary according to the following law:

$$V_o = \{ [(CONT + 6.93) / 69.3] * [(GAIN + 29.6) / 92.6] * 1.5 * V_{IN} \} + V_{REF+} \{ DC * 0.3 / 7 \}$$

Where:

$V_o$  is the output signal level

## LM1253 PREAMP+ OSD GENERATOR: V0.1



$V_{IN}$  is the input signal level before the AC coupling

$V_{REF}$  is the reference signal level

CONT is the Contrast register value (0-63)

GAIN is the Contrast register value (0-63)

DC is the DC register value (0-7)

From this it can be seen that the contrast control range is 20dB (10X) and the gain control range is 10dB (3.2X). The DC offset can vary the active video DC output level by 300mV in total, allowing a total range of adjustment of about 19.5V in eight 2.4V steps at the output of a typical AC<sub>2</sub>DC™ CRT driver.

The contrast and gain changes will operate immediately with changes in DAC value, as there is no filtering of the DAC outputs.

### 1.6 OSD TRANSFER CHARACTERISTIC

The nominal value of the OSD signal at the output shall vary according to the following law:

$$V_{O-OSD} = V_{OSD} * \{(GAIN + 29.6) / 92.6\} + V_{REF} + \{DC * 0.3 / 7\}$$

Where:

$V_{O-OSD}$  is the output signal level during OSD

$V_{OSD}$  is the internal OSD signal level from the OSD palette generator

$V_{REF}$  is the reference signal level

GAIN is the Contrast register value (0-63)

DC is the DC register value (0-7)

From this it can be seen that the OSD is not affected by the Brightness control, but is proportion to the Gain control, with a gain control range of 10dB (3.2X). The DC offset will affect the OSD output level by 300mV in total.

In order to provide smooth control of the video, all output parameters affected by digital controls must vary monotonically and smoothly, without any visible artifacts or glitches perceptible in the CRT image during adjustment.

NOTE: There should be no measurable variation in OSD level at the output with variations in bias or brightness control registers or contrast control register values, or with video input level.

**1.7 OSD BRIGHTNESS / BIAS TRANSFER CHARACTERISTIC**

The nominal value of the brightness / bias portion of the signal at the output during blanking shall vary according to the following law:

$$V_O = V_{REF} - \{BIAS * 0.50 / 63\} \\ - \{ ([BRIGHTNESS-31] * 0.20 / 63) * [(GAIN + 29.6) / 92.6] \} \\ - \{ PEDESTAL * 0.2 / 7 \}$$

Where :

$V_O$  is the output signal level during the blanking period

$V_{REF}$  is the reference signal level

BIAS is the Bias register value (0-63)

BRIGHTNESS is the Brightness register value (0-63)

GAIN is the Contrast register value (0-63)

PEDESTAL is the Pedestal register value (0-7)

From this it can be seen that the bias offset control range subtracts between 0 and 0.35v from the value of  $V_{REF}$  during blanking. The bias offset voltage is unaffected by changes in the other controls.

The brightness control range is bi-directional and adds or subtracts an additional amount between -0.2v and +0.2v from the value of  $V_{REF}$  during blanking, when gain is set between 0 and 63. This corresponds to a maximum brightness control range of about +/-14V at the CRT cathode.

The pedestal register controls the offset to the brightness control, in order that bi-direction operation of the brightness control is always possible at all bias voltage settings.

If gain is reduced, the brightness output voltage is reduced in proportion to allow gain tracking of the brightness control.

In order to provide smooth control of the video, all output parameters affected by digital controls must vary monotonically and smoothly, without any visible artifacts or glitches perceptible in the CRT image during adjustment.

NOTE 1: There should be no measurable variation in blanking level at the output with variations in contrast control register values, or with video input level.

**1.8 INTERNAL INTERFACE REQUIREMENTS****1.8.1 OSD SIGNAL**

The pre-amp interfaces internally with the OSD and I<sup>2</sup>C digital control circuitry. This part of the IC is defined in section 2 of this document.

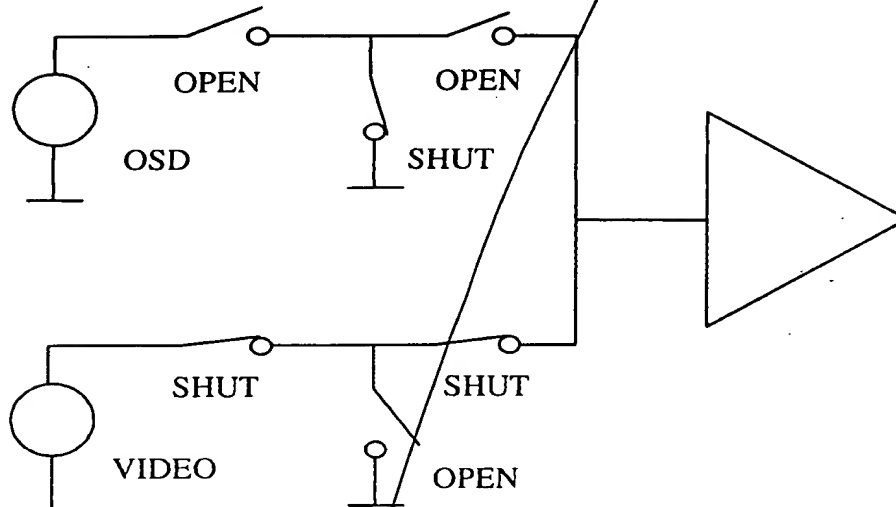
The digital and analog portions of the IC have separate external ground and Vcc connections and suitable layout considerations must be made to prevent digital noise from interfering in any way with the analog portion of the IC and vice versa.

The OSD signals are provided in analog format and originate within a 3 bit pallet DAC control block, which sets the amplitude depending upon the palette selected and the setting of the OSD I<sup>2</sup>C controlled contrast level.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
V <sub>OSDHIGH MAX</sub>	Typical      Maximum OSD high level	Palette set at max. OSD level Max		V <sub>ref</sub> + 1v		V
V <sub>OSDHIGH MIN</sub>	Typical      OSD      black level	Palette set at max. OSD level Max		V <sub>ref</sub>		V

**1.8.2 OSD CROSSTALK:**

Special care must be taken in the design of the analog switches that select between OSD and normal video in order to ensure that any cross talk between the video and the OSD is within the specified limits. This may require double attenuation switches such as shown conceptually below in to achieve the limits required in the specification table.



**Figure 7 DOUBLE SWITCHED OSD /VIDEO SOURCES FOR MINIMUM CROSSTALK**

## 1.9 EXTERNAL INTERFACE REQUIREMENTS

### 1.9.1 ABL CONTROL INPUT

The Auto Beam Limit control reduces the gain of the video amplifier in response to a control voltage proportional to the CRT beam current. This is required for CRT life and X-ray protection. The beam current limit circuit application is as shown in the figure below: when no current is being drawn by the EHT supply, current flows from the supply rail through the ABL resistor and into the ABL input of the IC. The IC clamps the input voltage to a low impedance voltage source.

When current is drawn from the EHT supply, the current passes through the ABL resistor, and reduces the current flowing into the ABL input of the IC.

When the EHT current is high enough, the current flowing into the ABL input of the IC drops to zero. This current level determines the ABL threshold and is given by:

$$I_{ABL} = \frac{V_S - V_{ABL\ TH}}{R_{ABL}}$$

Where:

$V_S$  is the external supply (usually the CRT driver supply rail (ie 80v)

$V_{ABL\ TH}$  is the threshold ABL voltage of the IC

$R_{ABL}$  is the ABL resistor value

$I_{ABL}$  is the ABL limit



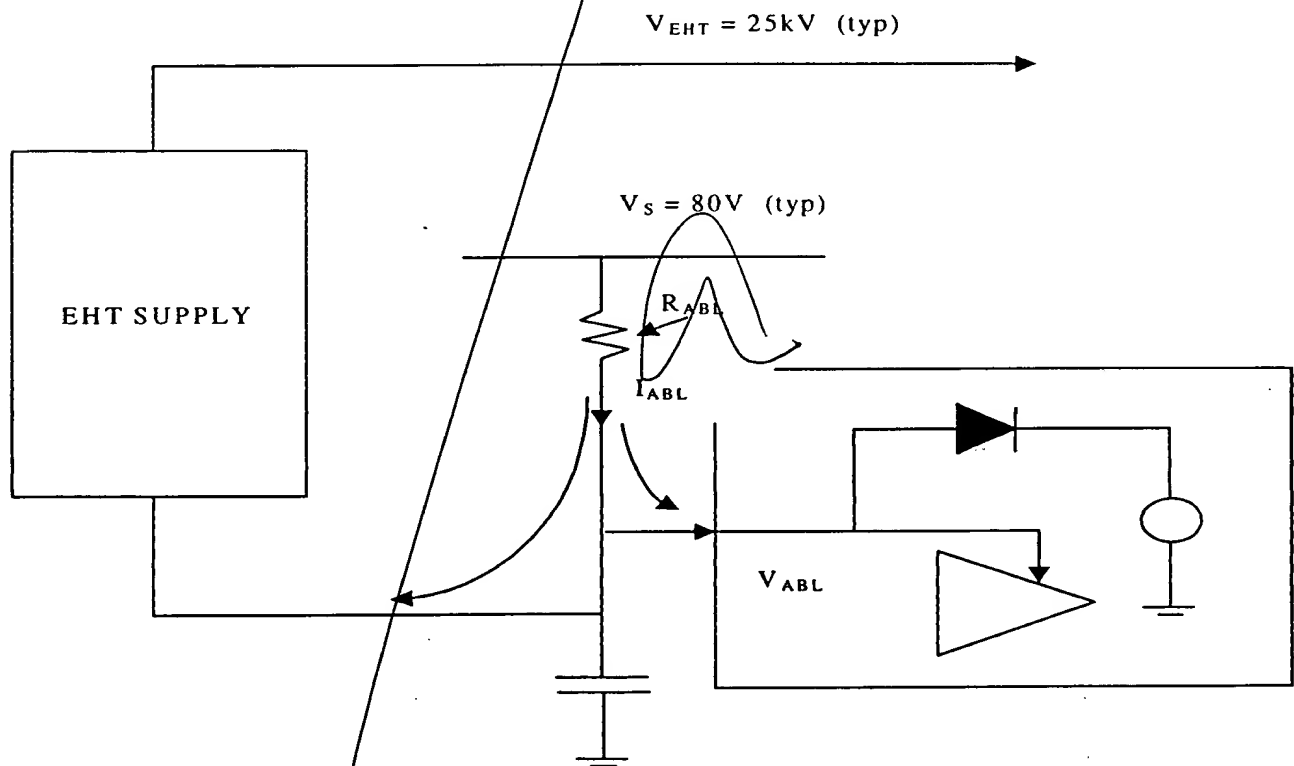
## LM1253 PREAMP+ OSD GENERATOR: V0.1

When the voltage on the ABL input drops below the ABL threshold of the pre-amp, the gain of the pre-amp reduces, which reduces the beam current. A feedback loop is thus established which acts to prevent the average beam current exceeding  $I_{ABL}$ .

The ABL input of the amplifier must act like a low impedance clamp to a constant voltage source while sinking current. When the ABL voltage drops below the threshold level, then the ABL input must appear as a very high impedance input, with negligible input bias current.

The ABL has two ranges of operation: over the initial range of approximately -5dB, the transfer characteristic of the preamplifier remains linear. This is sufficient for normal operation. Beyond -5dB of attenuation, the additional -5dB attenuation may result in some degradation of the linearity or frequency response of the LM1253.

Note that temperature drift characteristics while ABL is active (ie not at maximum gain) is not important, as the ABL control loop operates to maintain constant beam current.



### Figure 8 BASIC ABL CIRCUIT

## 15

## LM1253 PREAMP+ OSD GENERATOR: V0.1

## 1.10.3 AC PREAMP ELECTRICAL CHARACTERISTIC TARGETS AND LIMITS

Unless otherwise noted:  $V_{CC} = +5\text{ V}$ ,  $V_{IN} = 0.7\text{ VAC}$ ,  $C_L = 8\text{ pF}$ , Video signal output =  $1\text{ Vpp}$  at  $1\text{ MHz}$ ,  $T_C = 50\text{ }^\circ\text{C}$ ,  $V_{ref} = 1.80\text{ v}$ ,  $V_{ABL} = V_{CC}$  (See the figure below for Test Circuit)

## ACTIVE VIDEO SIGNAL PARAMETER TEST SETTINGS:

Test setting control values (unless other wise stated):

CONTROL:	NO. OF BITS	BASIC TEST SETTING 1	BASIC TEST SETTING 2	BASIC TEST SETTING 3	BASIC TEST SETTING 4
CONTRAST	6	MAX (Hex 3F)	MIN (Hex 00)	MAX (Hex 3F)	MAX (Hex 3F)
R,G,B GAIN	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	Set for 1v p-p on all channels
BRIGHTNES S	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	MIN (Hex 00)
R,G,B, BIAS	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	MIN (Hex 00)
VIDEO DC OFFSET	3	MIN (Hex 00)	MIN (Hex 00)	MAX (Hex 07)	MIN (Hex 00)

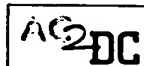
The following parameters are design targets and should be within the range or limits specified below: some limits may be specified in the data sheet.

Note: NA means not applicable

The following parameters apply to the active video portion of the waveform.

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## LM1253 PREAMP+ OSD GENERATOR: V0.1



Symbol	Spec Parameter	Conditions	Min	Target	Max	Units
$t_{PW\ CLAMP}$	Minimum clamp pulse width		200			ns
$V_{CLAMP\ MAX}$	Maximum low level clamp pulse voltage		1			V
$V_{CLAMP\ MIN}$	Minimum high level clamp pulse voltage		2.2		2.5	V
$V_{VBLANK\ HIGH}$	Minimum high level of vertical blank output	$V_{VREF\ BLANK} < 0.75V$	$V_{REF} + 1$			V
$V_{VBLANK\ LOW}$	Minimum output voltage of $V_{VBLANK}$ pin during Vertical blank	$I_{VBLANK\ OUT} = 100\mu A$			$V_{REF} - 1$	V
$t_{V\ BLANK}$	Typical vertical blanking Rise or Fall Time				1	$\mu S$
$t_{V\ BLANK - STRT\ PROP}$	Typical maximum vertical blanking start propagation delay	Reference $V_{VFLYBACK}$ input			200	ns
$C_{IP}$	Input AC coupling capacitor	Test Setting (4)			TBD	nF
$R_{IP}$	Minimum Typical Input resistance	Test Setting (4)		20		Meg Ohm
	Thermal Smear	Tested in Monitor with NSC Neck Board and AC <sub>2</sub> DC™ Driver			None Visible	
$V_{ref}$	Typical Vref output voltage		1.75	1.8	1.85	V
$V_{ref\ I_{max}}$	Maximum operational sourced output current of $V_{ref}$		300	NA	NA	$\mu A$

Note 1: Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Linearity Error is the variation in step height of a 16 step staircase input signal waveform with 0.7vp-p level at the input, subdivided into 16 equal steps, with each step approximately 100ns in width.

LM1253 PREAMP+ OSD GENERATOR: V0.1

**Note 5:** Input from signal generator:  $t_r, t_f < 1 \text{ ns}$ .

**Note 6:** ABL should provide smooth decrease in gain over the operational range of 0db to -5db

$$\Delta A_{ABL} = A(V_{ABL} = V_{ABL \text{ MAX GAIN}}) - A(V_{ABL} = V_{ABL \text{ MIN GAIN}})$$

Beyond  $-5\text{db}$  the gain characteristics, linearity and pulse response may depart from normal values.

#### 1.10.4 BRIGHTNESS/BIAS SIGNAL PARAMETER TEST SETTINGS

The following specification parameters apply to the test of the brightness / bias portion of the waveform.

Test setting control values (unless otherwise stated):

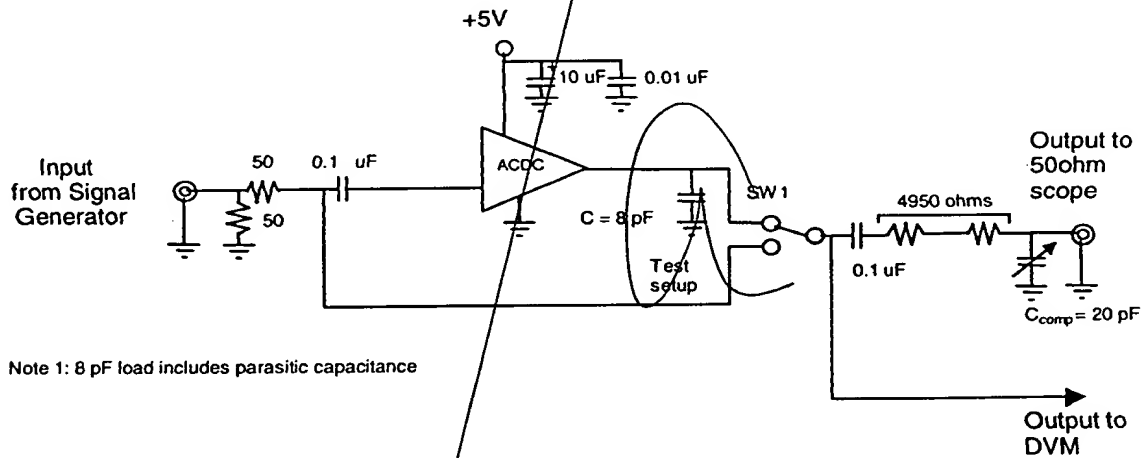
CONTROL:	NO. OF BITS	BASIC TEST SETTING 5	BASIC TEST SETTING 6	BASIC TEST SETTING 7	BASIC TEST SETTING 8
CONTRAST	6	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)	MAX (Hex 3F)
R,G,B GAIN	6	MAX (Hex 3F)	MIN (Hex 00)	MAX (Hex 3F)	MAX (Hex 3F)
BRIGHTNESS	6	MAX (Hex 3F)	MAX (Hex 3F)	MIN (Hex 00)	MIN (Hex 00)
R,G,B, BIAS	6	MAX (Hex 3F)	MIN (Hex 00)	MAX (Hex 3F)	MIN (Hex 00)
VIDEO OFFSET	DC 3	MIN (Hex 00)	MIN (Hex 00)	MIN (Hex 00)	MIN (Hex 00)
PEDESTAL OFFSET	3	MAX (Hex 07)	MAX (Hex 07))	MAX (Hex 07)	MIN (Hex 00)

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1.10.5 BRIGHTNESS/BIAS SIGNAL PARAMETER SPECIFICATIONS:

The following parameters apply to the brightness /bias portion of the output waveform.

Symbol	Spec Parameter	Conditions				Units
			Min	Target	Max	
$V_{\text{BLANK MAX TYP}}$	Typical Maximum blanking level	Test Setting (5)		$V_{\text{REF}} - 0.90$		V
$V_{\text{BLANK MIN}}$	Minimum blanking level	Test Setting (8)		$V_{\text{REF}}$		V
$t_{\text{BLK rtyp}}$	Typical Blanking Rise Time	Test Setting (5), 10% to 90%,		30		nS
$t_{\text{BLK ftyp}}$	Typical Blanking Fall Time	Test Setting (5), 10% to 90%,		30		nS



**Figure 9 TEST CIRCUIT (ONE CHANNEL)**

The above figure shows a typical test circuit for evaluation of the LM1253 preamp. This circuit is designed to allow testing of the AC<sub>2</sub>DC™ preamp in a 50-ohm environment without the use of an expensive FET probe. The 4950 ohm resistor at the output forms a 100:1 voltage divider when connected to a 50 ohm load. Ccomp must be adjusted for flat response with SW1 in test setup position.

## 2 ANALOG/DIGITAL INTERFACE

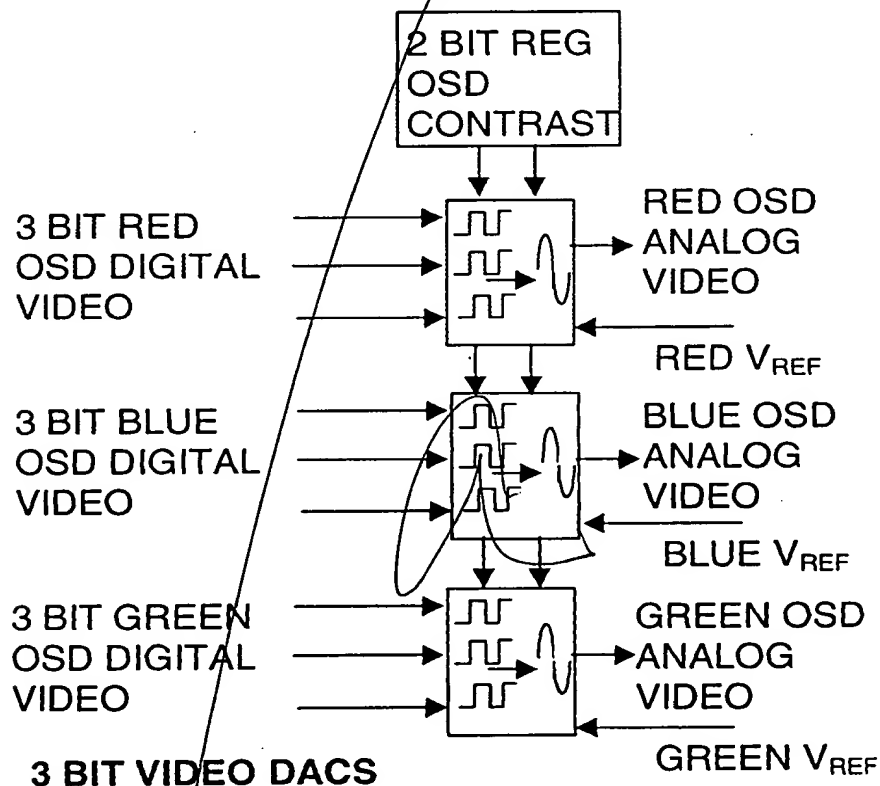
### 2.1 OSD VIDEO DAC

#### 2.1.1 OSD DAC BASIC OPERATION

The OSD DAC is controlled by the 9 bit (3x3bits) OSD video information coming from the pixel serializer register (see also section 1 and section 3).

The OSD DAC is shown conceptually in the figure below, where the gain is programmable by the 2bit OSD CONTRAST register, in 4 stages to give the required peak OSD signal as specified in section 1.

The OSD DACs uses the internal reference voltage,  $V_{ref}$ .



**Figure 10 BLOCK DIAGRAM OF OSD DACS**

The OSD DAC creates the analog signal biased with respect to the reference voltage. The DAC must be monotonic and linear. The full scale output voltage with an OSD video input of '111' and a maximum contrast setting of '11' should be nominally 1v.



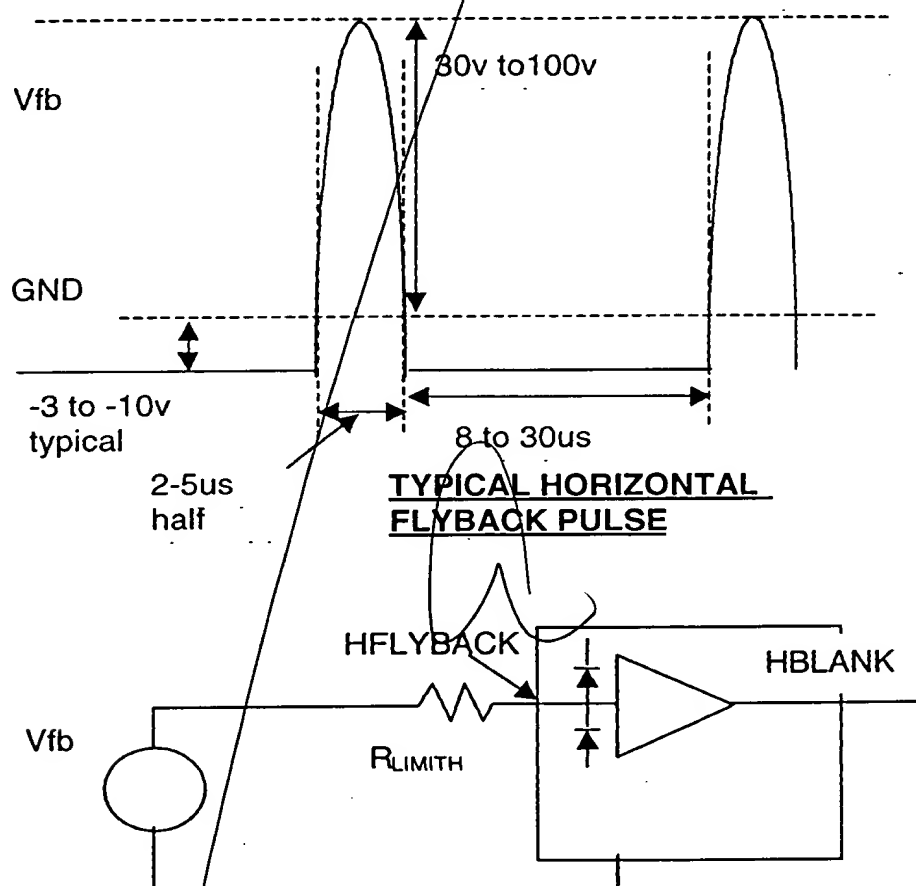
## LM1253 PREAMP+ OSD GENERATOR: V0.1

**2.2 ANALOG / DIGITAL EXTERNAL INTERFACE SIGNALS**

These signals are presented to the digital section of the IC at the external interface to the monitor system via the device pins:

**2.2.1 HFLYBACK:**

HFLYBACK is an analog signal input from the monitor horizontal scan. HBLANK is digital signal derived from the horizontal flyback pulse shaped as per the figure below:

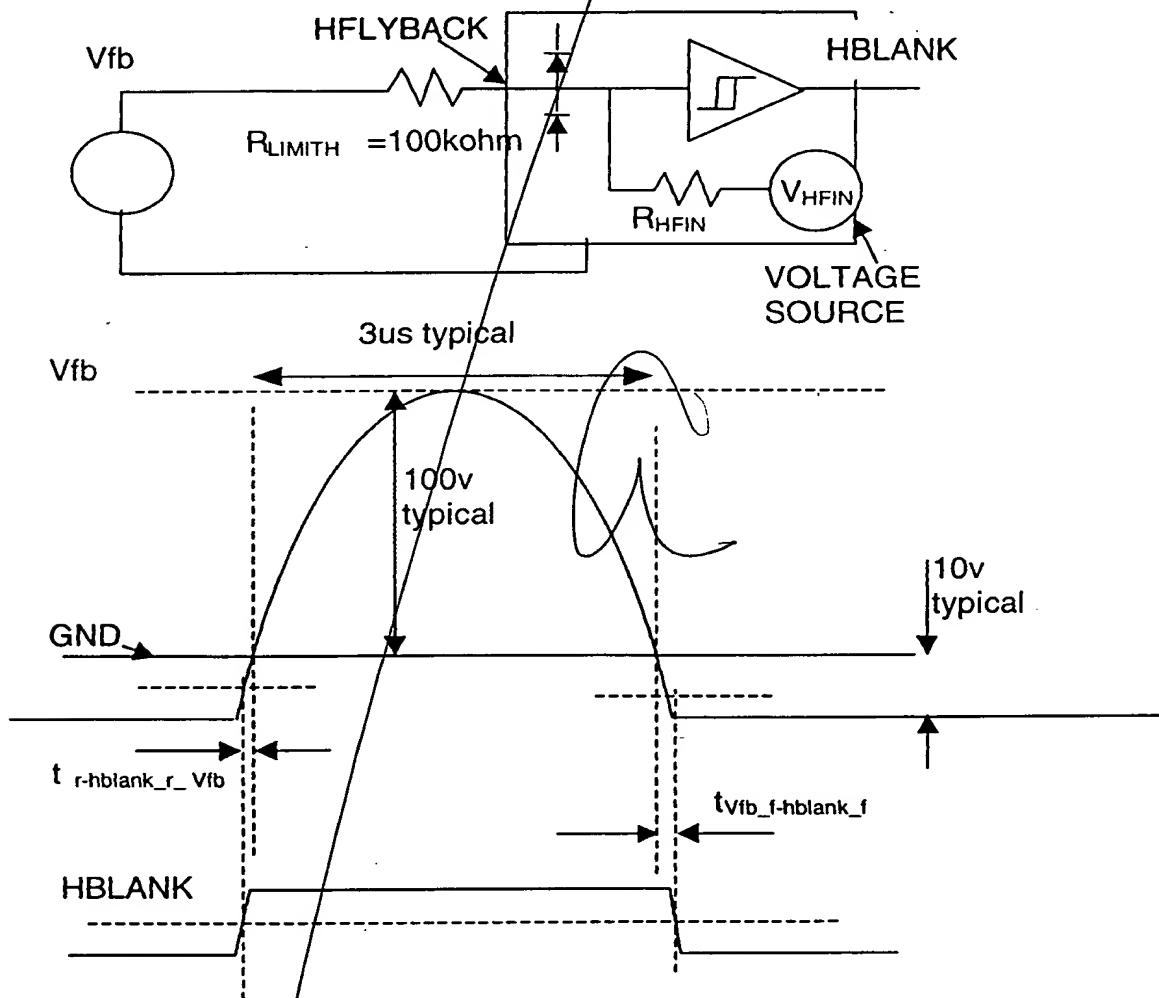


**Figure 11 HFLYBACK INPUT PULSE**

$R_{LIMITH}$  is set to limit the input current into the IC to a maximum value of +2mA during flyback and -150uA during normal forward scan. The internal input impedance of the I/O ( $R_{HFIN}$ ) is low to limit the maximum voltage swing at the input to within the supply rail and ground. The IC interface circuit creates a digital signal from this waveform, which is used as the blanking signal, and termed HBLANK. This signal is used by the video amplifier for blanking the video, and by the OSD generator as the horizontal sync reference for the PLL.

The PLL will detect if no signal is present at the input for any sustained period. When no signal is present, the PLL will produce a signal to set the video output level to the black level.

$R_{LIMITH}$  shall be as large as possible (nominally 100kohm).



**Figure 12 TEST CONDITIONS FOR HBLANK SIGNAL**

The input should have voltage excursion clamps to prevent the input being damaged by excessive input voltage swing. The HBLANK line should normally trigger high when the rising edge of the flyback pulse has passed through the AC zero level. It should

normally trigger low within 100ns of the flyback signal falling below the AC zero volt level.

PARAMETER	SYMBOL	MIN	TARGET	MAX
HBLANK rising edge to Flyback signal rising edge zero crossing point	$t_{r-hblank\_r\_vfb}$			
Flyback signal falling edge zero crossing point to HBLANK falling edge	$t_{vfb\_f-hblank\_f}$		0	
$I_{OUT}$ HBLANK detection threshold	$I_{TH}$		-20uA	
Minimum normal forward scan current at lowest horizontal frequency that will ensure HBLANK signal will activate normally	$I_{IN-MIN}$		-30uA	
Maximum normal forward scan current at lowest horizontal frequency that input can withstand	$I_{IN-MAX}$		TBD	
Maximum flyback scan current @ 125kHz that input can withstand	$I_{IN+MAX}$		TBD	

### 2.2.2 VFLYBACK:

This is an analog signal from the monitor vertical scan. The analog waveform is AC coupled if necessary to remove the low frequency and DC components. This signal is fed to the input of the IC via a current limiting resistor to prevent the positive and negative excursions of the signal causing excessive current or voltage swing at the input to the IC.

$R_{LIMITV}$  is set to limit the maximum input voltage swing into the IC to less than the supply rails. The input stage is a voltage source  $V_{VFIN}$  with an input resistance of  $R_{VFIN}$ . The input to the IC is positive edge triggered, and ignores the falling edge. Because of horizontal rate noise on the waveform, the input buffer incorporates hysteresis, triggering at a positive going threshold of  $V_{VTH+}$  and a negative going threshold of  $V_{VTH-}$ . The input should have very low bias current (<50uA) due to the high source impedance, and should have ESD clamps to prevent the input being damaged by excessive input voltage swing.

The input buffer produces a digital signal VSTART which is used to start the VBLANK timer. The positive rising edge of VSTART sets a counter timer, which counts horizontal periods using the HBLANK signal. The timer resets VBLANK when it reaches the value preset in the register VCOUNT (set by the micro-controller over  $I^2C$ ).

While the output VBLANK is active, an AND function prevents any further transitions on the VSTART waveform from retriggering the counter.

The end of the VBLANK pulse should not dither between lines (causing 1line vertical jumping) due to slight variations in the phase of VFLYBACK and HBLANK.

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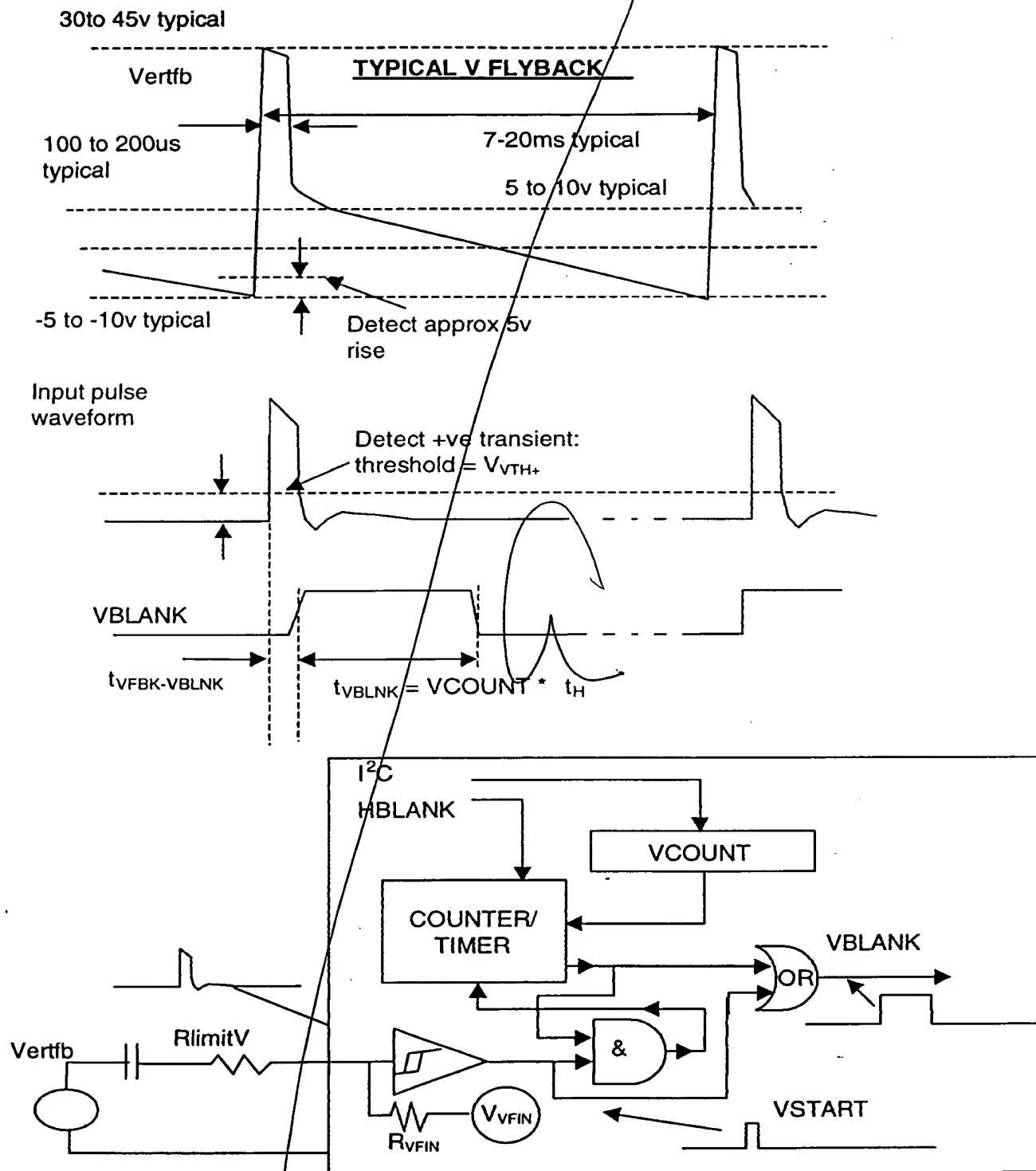


Figure 13 VERTICAL FLYBACK INPUT PULSE

# LM1253 PREAMP+ OSD GENERATOR: V0.1



PARAMETER	SYMBOL	MIN	TARGET	MAX
Vertical flyback signal rising edge to VBLANK rising edge	$t_{Vfb\_r-hblank\_r}$		<1us	
VBLANK duration	$t_{VBLNK}$		(VCOUNT) * $t_H$	
VFLYBACK input voltage source	$V_{VFIN}$		$0.25 * V_{CC}$	
VFLYBACK input voltage source resistance	$R_{VFIN}$		8k	
VFLYBACK positive detection going threshold	$V_{VTH+}$		$V_{VFIN} + 500mV$	
VFLYBACK negative detection going threshold	$V_{VTH-}$		$V_{VFIN} + 150mV$	

## 2.2.3 LOSS OF VERTICAL FLYBACK PULSE

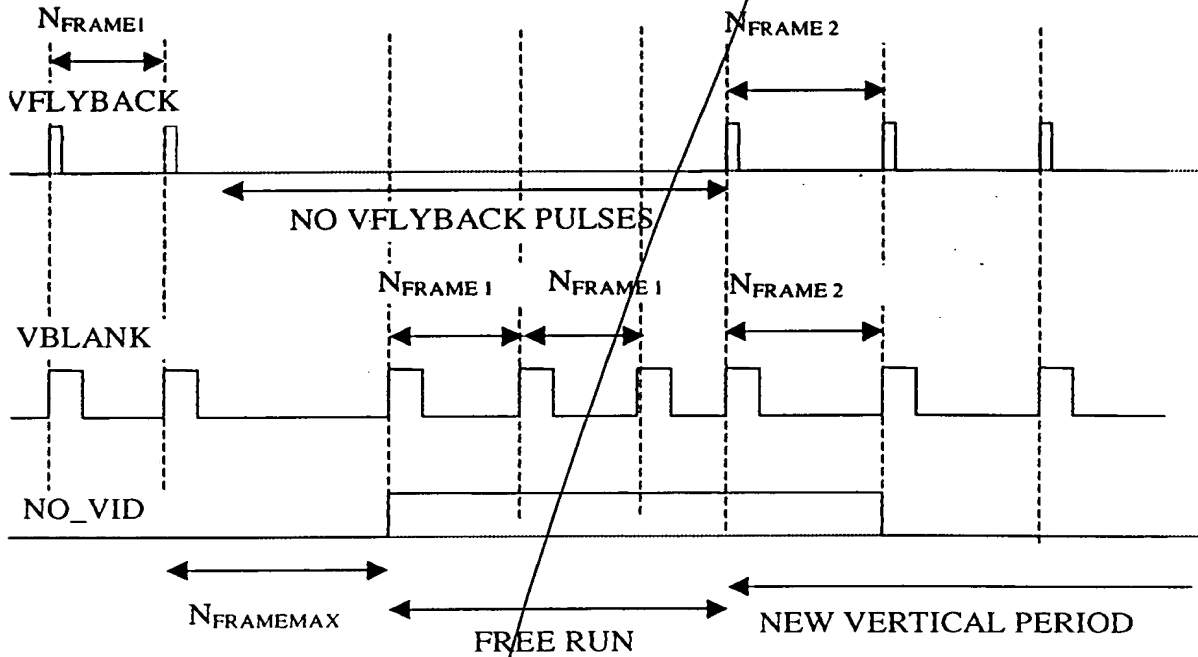
Loss of vertical flyback pulse implies that the monitor is not scanning, and therefore no image is being displayed. The HBLANK and VBLANK pulses are still required by the AC<sub>2</sub>DC™ driver in order to maintain correct bias conditions in the CRT until the power supplies are switched off, but video should be set at black level to prevent front of screen problems.

Loss of vertical flyback will be detected when the frame line counter runs past the previously stored frame line count,  $N_{FRAME}$  by more than two lines. The two lines allows for some error in the counting of the number of lines in the frame due to noise on the VFLYBACK pulse.

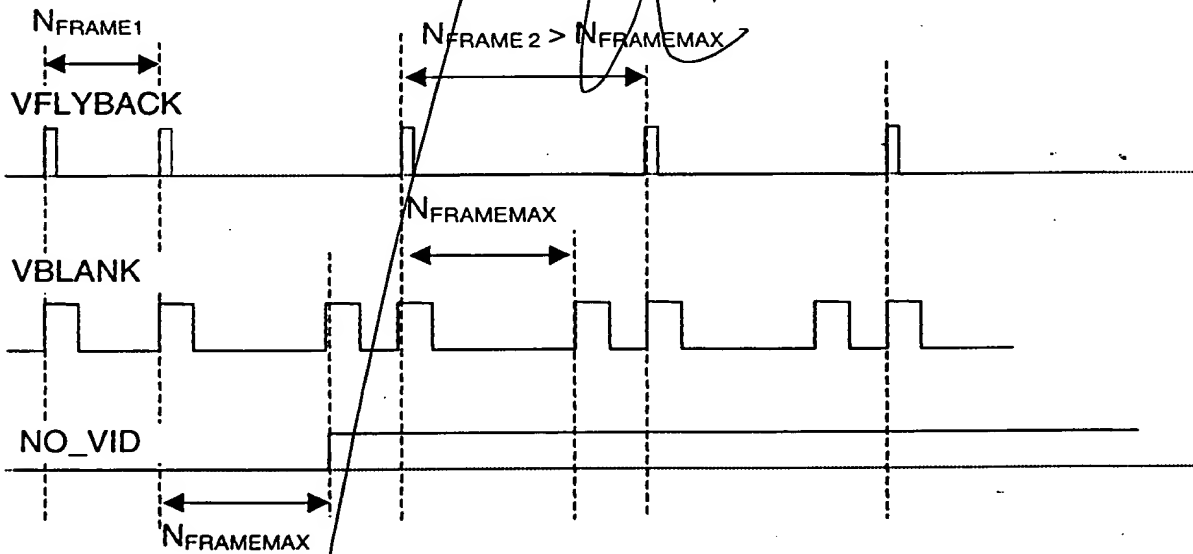
Note also that interlace mode is supported by the LM1253. In interlace mode, a frame is composed of two sequential fields. In the first field, the odd lines are displayed. In the second field the even lines are displayed. A complete frame consists of an odd number of horizontal lines, so that each field contains a half line. This will result in an alternate half line phase difference between each field of the VFLYBACK pulse with respect to the HBLANK pulse.

Note that the blanking circuit will only detect the absence of a vertical flyback pulse. In that case it will free run at a period of  $N_{FRAME} * t_H$ . It will not reliably detect or blank the video if an erratic pulse occurs.

Examples of the operation of the VBLANK signal are shown below. Note: the change from one vertical frequency to another is sometimes continuous, with no break in VFLYBACK pulses.



**Figure 14** EXAMPLE1: OPERATION WHEN FRAME PERIOD CHANGES  
FROM  $N_{FRAME1}$  TO  $N_{FRAME2}$



**Figure 15** EXAMPLE2: OPERATION WHEN FRAME PERIOD CHANGES  
FROM  $N_{FRAME1}$  TO  $N_{FRAME2}$ , WHERE  $N_{FRAME2} > N_{FRAMEMAX}$

## 2.3 HORIZONTAL PHASE LOCKED LOOP

### 2.3.1 LOSS OF HORIZONTAL FLYBACK PULSE

Loss of horizontal flyback pulse implies that the monitor is not scanning, and therefore no image is being displayed. The HBLANK pulse is still required by the AC<sub>2</sub>DC™ driver in order to maintain correct bias conditions in the CRT until the power supplies are switched off, but video should be set at black level to prevent front of screen problems.

In the absence of an externally supplied horizontal flyback pulse, the PLL will free run and generate its own HBLANK pulse at a frequency of  $F_{\text{FREE\_RUN}}$  after a number of missed horizontal line periods,  $N_{\text{MISSED}}$ . The PLL free run pulse will be gated into the HBLANK line to the pre-amp to allow normal operation of the pre-amp and driver biasing. The free run pulse width will be between 1/8 and 1/16<sup>th</sup> of the horizontal period.

PARAMETER	SYMBOL	MIN	MAX
HORIZONTAL PERIOD	$t_H$	20kHz	125kHz
NO. OF PIXELS PER LINE	$N_H$	HCOUNT	HCOUNT+32
PIXEL CLOCK FREQUENCY	$F_P$	6.4MHz	96MHz
JITTER	$t_{\text{JITTER}}$	-	0.025% of $t_H$
DRIFT	$dF_{\text{DRIFT}}$	-	2%
FREE RUN HBLANK FREQUENCY	$F_{\text{FREE\_RUN}}$	30kHz	60kHz
MISSING H PERIODS BEFORE FREE RUN FREQUENCY	$N_{\text{MISSED}}$		10
MAXIMUM CAPTURE AND SETTLING TIME IN NUMBER OF H PERIODS AFTER CHANGE IN H FREQUENCY	$N_{\text{SETTLE}}$	0	512

The PLL clock frequency will drift by no more than  $dF_{\text{DRIFT}}$  over the device operating temperature range.

### 2.4 VCC DETECT:

The Vcc power supply will be continuously monitored. Should the Vcc supply drop to less the  $V_{\text{CCDET}}$  then the LM1253 will set the output video to  $V_{\text{REF}}$ .

The device should continue to operate down to  $V_{\text{CCDET}}$ , although some parameters may fall outside of specification when the supply drops below  $V_{\text{CCMIN}}$ .



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AC<sub>2</sub>DC

PARAMETER	SYMBOL	MIN	MAX
Vcc undervoltage detection threshold	V <sub>CCDET</sub>	4.0V	4.25V

a

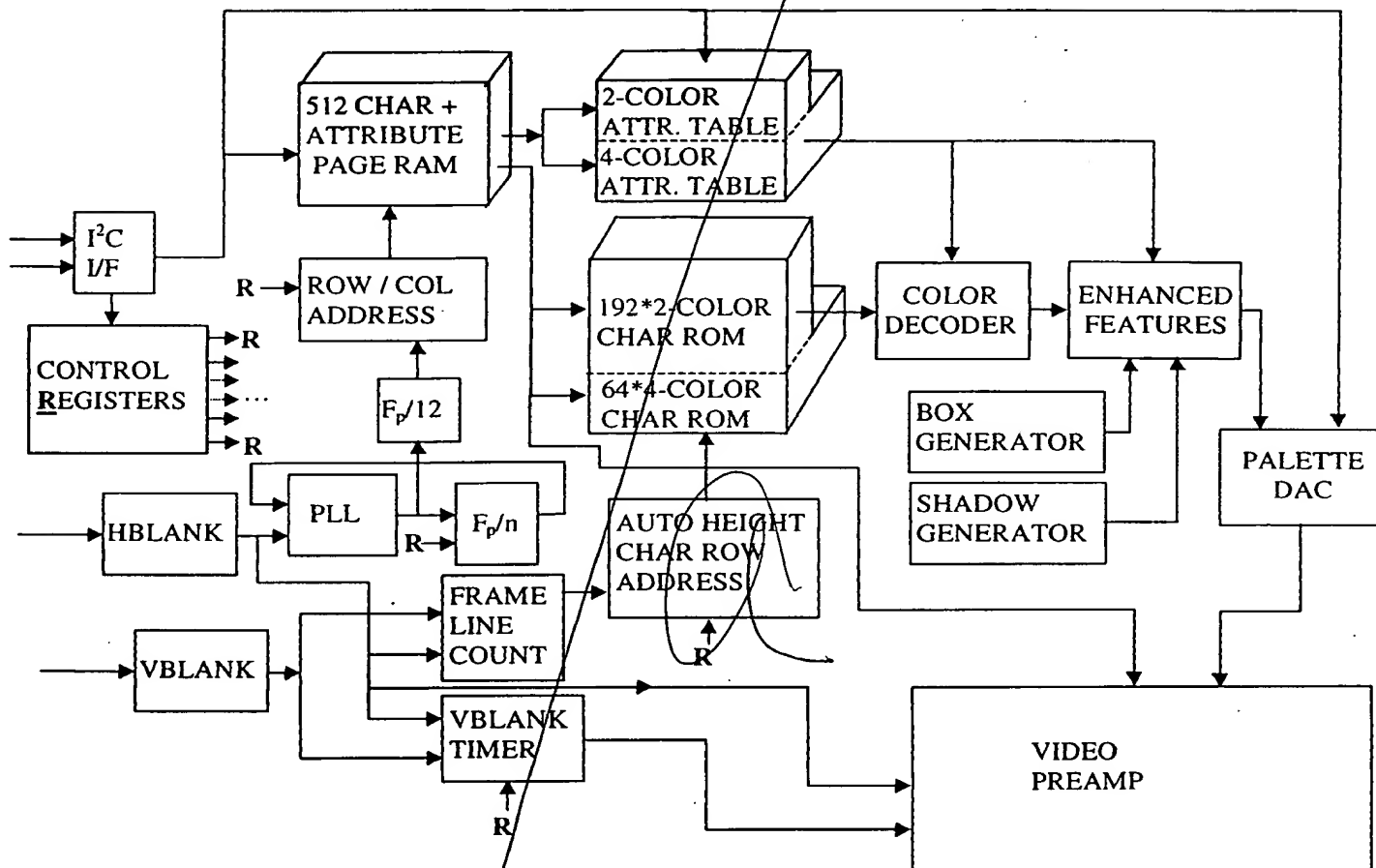
004201" 6E786960

### 3 OSD GENERATOR

#### 3.1 OSD GENERATOR OPERATION

##### 3.1.1 PAGE OPERATION

The block diagram of the OSD generator is shown in the figure below:



**Figure 16 BLOCK DIAGRAM OF THE OSD GENERATOR**

Video information is created using any of the 256 pre-defined characters stored in the mask programmed ROM. Each character has a unique 8 bit code that is used as its address. Consecutive rows of characters make up the displayed window. These characters can be stored in the page RAM, written under I<sup>2</sup>C controlled commands by the monitor micro-controller. Each row can contain any number of characters up to the limit of the displayable line length, although some restrictions concerning the enhanced features apply on character rows longer than 32 characters.

The number of characters across the width and height of the page can be varied under I<sup>2</sup>C control, but the total number of characters that can be stored and displayed on the

screen is limited to 512 including any character row end characters. The horizontal and vertical start position can also be programmed under I<sup>2</sup>C control.

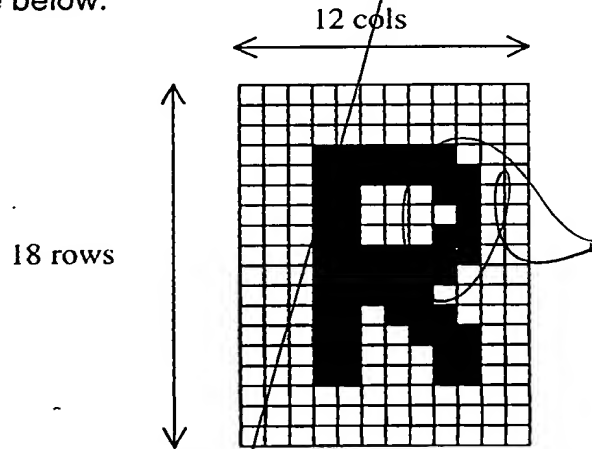
### 3.1.2 WINDOWS

Two separate windows can be opened, utilizing the data stored in the page RAM. Each window has its own horizontal and vertical start position, although the second window should be horizontally spaced at least two character spaces away from the first window.

### 3.1.3 CHARACTER CELL

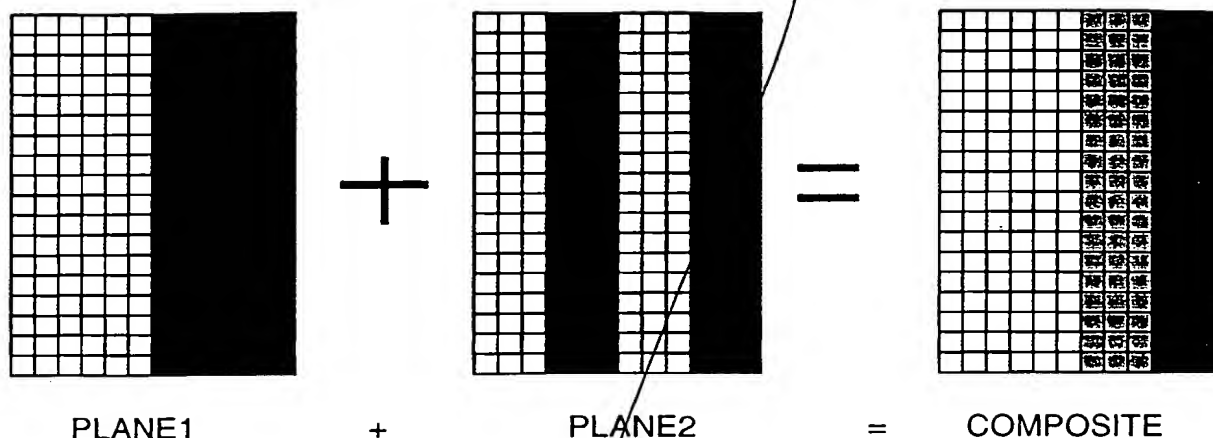
Each character is defined as a 12 wide by 18 high matrix of picture elements, or 'pixels'. There are two types of characters defined in the character ROM:

- i. **Two-color:** there are 192 two-color characters. Each pixel of these characters is defined by a single bit value. If the bit value is 0, then the color is defined as 'Color 1' or the 'background' color. If the bit value is 1, then the color is defined as 'Color 2', or the 'foreground' color. An example of a character is shown in the figure below:



**Figure 17 A TWO-COLOR CHARACTER**

- ii. **Four-color:** there are 64 four-color characters stored in the character ROM. Each pixel of the four-color character is defined by two bits of information, and thus can define four different colors, Color1, Color2, Color3, Color4. Color 1 is defined as the 'back ground' color. All other colors are considered 'foreground' colors, although for most purposes, any of the four colors may be used in any way. Because each four-color character has two bits, the matrix has two planes of ROM.



**Figure 18 A FOUR COLOR CHARACTER**

### 3.1.4 ATTRIBUTE TABLES

Each character has an attribute value assigned to it in the page RAM. The attribute value is 4 bits wide, making each character entry in the page RAM 12 bits wide in total. The attribute value acts as an address which points to one of 16 entries in either the two-color attribute table RAM or the four-color attribute table RAM. The attribute word in the table contains the coding information which defines which color is represented by color1 and color2 in the two color attribute table and color1, color2, color3, color4 in the four-color attribute table. Each color is defined by a 9bit value, with 3bits assigned to each channel of RGB. A dynamic look up table defines each of the 16 different color combination selections or 'palettes'. As the look up table can be dynamically coded by the micro-controller over the I<sup>2</sup>C interface, each color can be assigned to any one of 2<sup>9</sup> (i.e. 512) choices. This allows a maximum of 64 different colors to be used within one page using the 4-color characters, with up to 4 different colors within any one character. and 32 different colors using the 2-color characters, with 2 different colors within any one character.

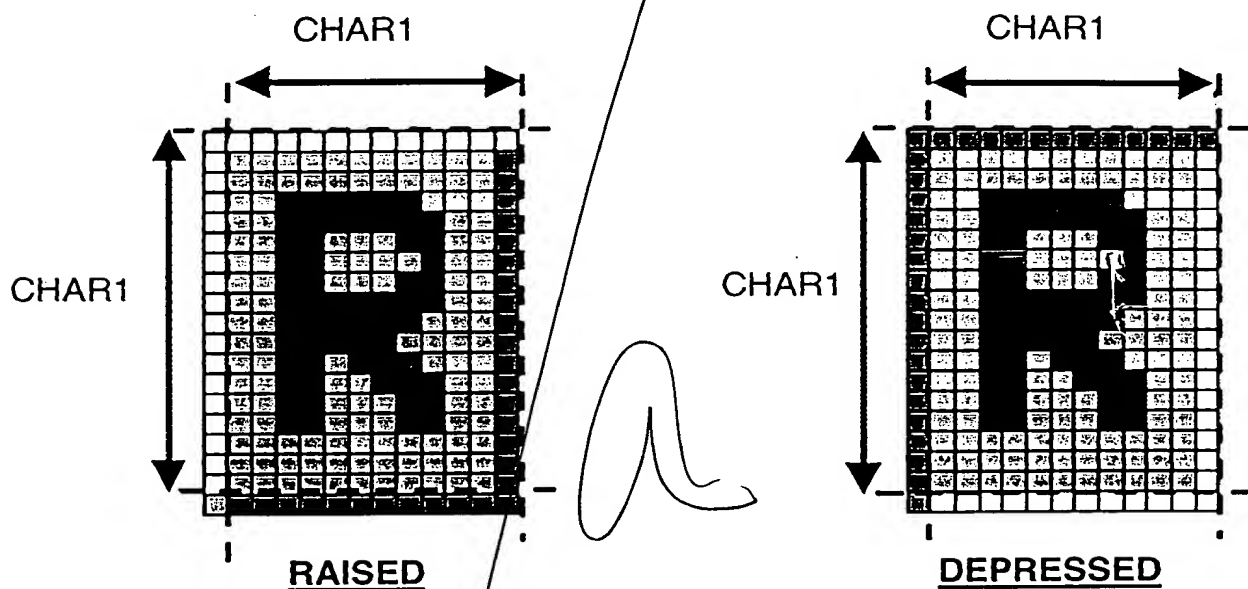
### 3.1.5 TRANSPARENT DISABLE

In addition to the 9 lines of video data, a tenth data line is generated by the transparent disable bit. When this line is activated, the black color code will be translated as 'transparent' or invisible. This allows the video information from the PC system to be visible on the screen when this is present. Note that this feature is only enabled on Color 1 of the first 8 attribute table entries, in order to allow some black color palettes to be used in combination with the transparent feature.

### 3.1.6 ENHANCED FEATURES

In addition to the wide selection of colors for each character, additional character features can be selected on character by character basis.

- i. Windows95™ style button boxes. The OSD generator examines the character string being displayed and if the 'button box' attributes have been set in the Enhanced feature byte, then a box creator selectively substitutes the character pixels in either or both the top and left most pixel line or column with a button box pixel.



Effect on the screen:

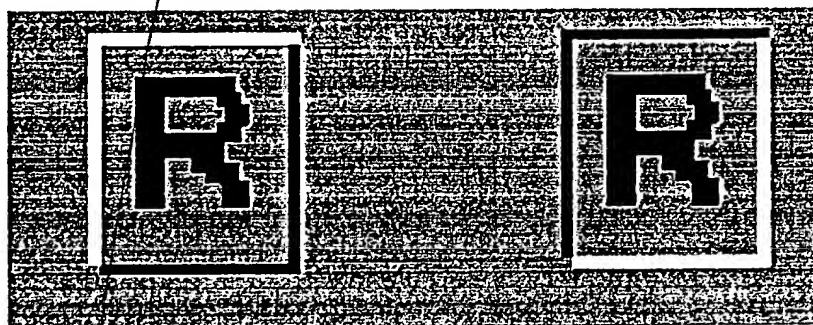
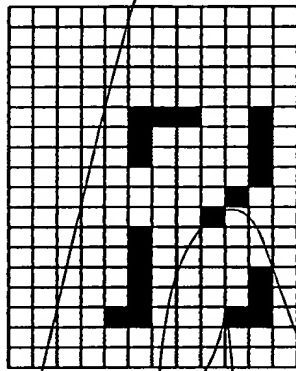


Figure 19 WINDOWS95™ STYLE 'BUTTON BOXES'

The shade of the button box pixel depends upon whether a 'depressed' or 'raised' box is required, and can be programmed by I<sup>2</sup>C. The raised pixel color ('highlight') is defined by the value in the color palette register, EF1 (normally white). The depressed pixel ('lowlight') color by the value in the color palette register EF2 (normally gray).

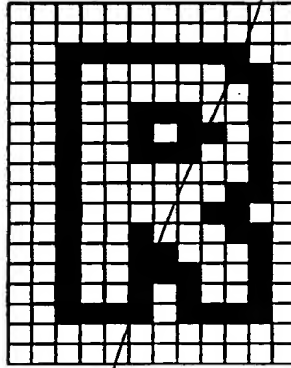
- ii. Heavy Button Boxes  
When heavy button boxes are selected, the color palette value stored in register EF3 is used for the depressed ('lowlight') pixel color instead of the value in register EF2.
- iii. Shadowing: shadowing can be added to two-color characters by choosing the appropriate attribute value for the character. When a character is shadowed, a shadow pixel is added to the lower right edges of the color2 image, as shown in the figure below:



**Figure 20 SHADOWING**

The color of the shadow is determined by the value in the color palette register EF3 (normally black).

- iv. Bordering: a border can be added to the two-color characters. When a character is bordered, a border pixel is added at every horizontal, vertical or diagonal transition between color1 and color2.



**Figure 21 BORDERING**

The color of the border is determined by the value in the color palette register EF3 (normally black).

- v. Blinking: if blinking is enabled as an attribute, all colors within the character except the button box pixels which have been over-written will alternately switch to color1 and then back to the correct color at a rate determined by the micro-controller under I<sup>2</sup>C control.

### 3.2 MICRO-CONTROLLER INTERFACE

The micro-controller interfaces to the AC/DC Pre-Amp via an I<sup>2</sup>C interface. The protocol of the interface begins with a Start Pulse followed by a seven bit Slave Device Address and a Read/Write bit. Each I<sup>2</sup>C Slave Device decodes its own address and responds to all reads and writes to that address. The address associated with the AC/DC Pre-Amp is *TBD*.

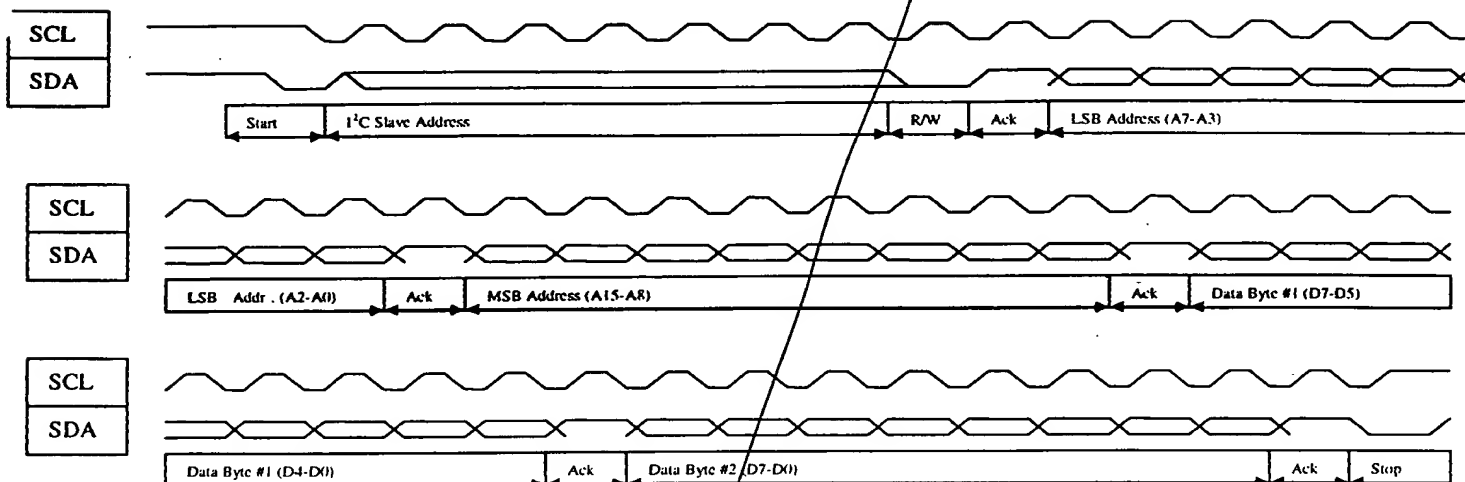
The figures below show a write and read sequence across the I2C interface.

#### 3.2.1 WRITE SEQUENCE

Following the Start Pulse, the Slave Device Address, the Read/Write bit (a zero, indicating a write) and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit.

The next 8-bits will be the write data associated with the address indicated by the two address bytes. Subsequent write data bytes will correspond to the next increment address locations

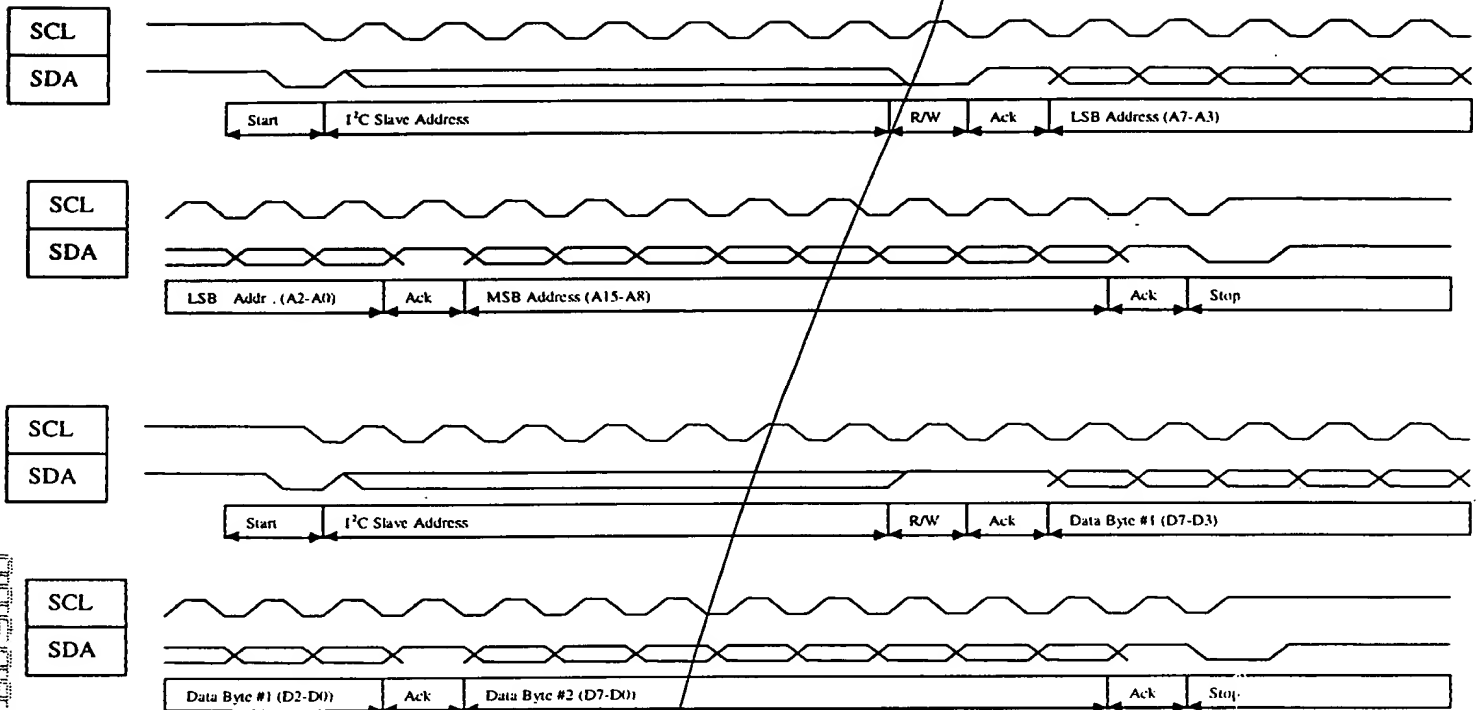
## LM1253 PREAMP+ OSD GENERATOR: V0.1

**Figure 22 I<sup>2</sup>C WRITE SEQUENCE****3.2.2 READ SEQUENCE**

Read sequences are comprised of two I2C transfer sequences: The first being a write sequence that only transfers the two byte address to be accessed. The second being a read sequence that starts at the address transferred in the previous address only write access and incrementing to the next address upon every data byte read.

The following timing diagram illustrates an entire read sequence:





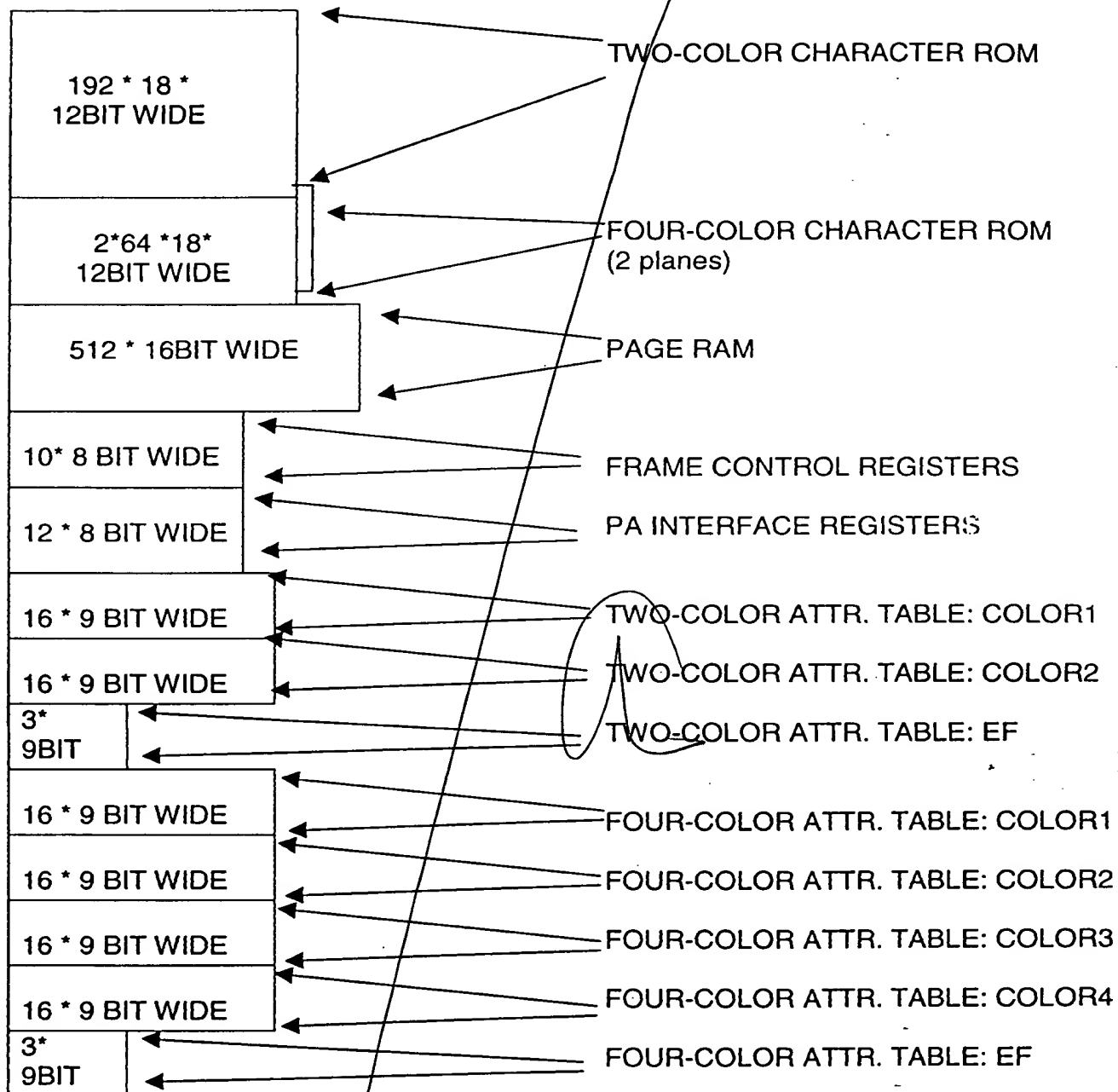
**Figure 23 I<sup>2</sup>C READ SEQUENCE**

Following the Start Pulse, the Slave Device Address, the Read/Write bit (a zero, indicating a write) and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access.

Next the read data access will be performed beginning with the Start Pulse, the Slave Device Address, the Read/Write bit (a one, indicating a read) and the Acknowledge bit; Then the next 8-bits will be the read data driven out by the AC/DC Pre-Amp associated with the address indicated by the two address bytes. Subsequent read data bytes will correspond to the next increment address locations.

### 3.3 I<sup>2</sup>C IC ADDRESS

The slave address of the LM1253 is 5D.

**3.4 I<sup>2</sup>C AC/DC PRE-AMP ADDRESS MAP****3.4.1 ROM, RAM AND REGISTERS ADDRESSED BY I<sup>2</sup>C**

## 3.4.2 CHARACTER ROM

Address Range	R/W	Description
0000h – 2FFFh	R	<p>ROM Character Fonts, 192 two-color Character Fonts that are Read-Only.</p> <p>The format of the address is as follows:</p> <p>A15-A14: Always zeros.</p> <p>A13-A6: Character value (00h – BFh are valid values)</p> <p>A5-A1: Row of the character (00h-11h are valid values)</p> <p>A0: Low byte of line when a zero. High byte of line when a one.</p> <p>The low byte will contain the first eight pixels of the line with data Bit 0 corresponding to the left most bit in the Character Font line. The high byte will contain the last four pixels and data Bits 7-4 are "don't cares". Data Bit 3 of the high byte corresponds to the right most pixel in the Character Font line.</p>
3000h – 3FFFh	R	<p>ROM Character Fonts, 64 four-color Character Fonts that are Read-Only.</p> <p>The format of the address is as follows:</p> <p>A15-A14: Always zeros.</p> <p>A13-A6: Character value (C0h – FFh are valid values)</p> <p>A5-A1: Row of the character (00h-11h are valid values)</p> <p>A0: Low byte of line when a zero. High byte of line when a one.</p> <p>The low byte will contain the first eight pixels of the line with data Bit 0 corresponding to the left most bit in the Character Font line. The high byte will contain the last four pixels and data Bits 7-4 are "don't cares". Data Bit 3 of the high byte corresponds to the right most pixel in the Character Font line.</p> <p>NOTE: The value of Bit 0 of the Character Font Access Control Register (I2C Address 8402h) is a zero, it indicates that the Bit 0 data value of the four-color pixels is being accessed via these addresses. When the value of Bit 0 of the Access Control Register is a one, it indicates that the Bit 1 data value of the four-color pixel is being accessed via these addresses.</p>
4000h – 7FFFh		RESERVED.

## 3.4.3 DISPLAY PAGE RAM

Address Range	R/W	Description
8000h – 81FF	R/W	Display Page RAM Characters. A total of 512 display characters, skipped line, end-of-row and end-of-window character codes may be supported via this range.  To support skipped lines and character attributes a number of special case rules are used when writing to this range. (Refer to the Display Page RAM section of this document for more details.)

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## LM1253 PREAMP+ OSD GENERATOR: V0.1

## 3.4.4 PRE-AMP INTERFACE REGISTERS

LM1253 OSD Interface Registers											
Register	Address	Reset	D7	D6	D5	D4	D3	D2	D1	D0	
Fonts-2color	0000-2FFE		PIXEL[7:0]								
	+1		PIXEL[11:8]								
Fonts-4color	3000-3FFE		PIXEL[7:0]								
	+1		PIXEL[11:8]								
Display Page	8000-83FF		CHAR_CODE[7:4] or reserved				CHAR_CODE[3:0] or ATTR_CODE				
FRMCTRL1	8400	10	TD			CDPR	D2E	D1E	OSE		
FRMCTRL2	8401	80	PIXELS PER LINE[2:0]			BLINK PERIOD[4:0]					
CHARFONTACC	8402	00	ATTR							FONT4	
VBLANKDUR	8403	10	VBLANK_DURATION[6:0]								
CHARHTCTRL	8404	51	CHAR_HEIGHT[7:0]								
BBHLCTRLB0	8405	FF	R[1:0]		B[2:0]			G[2:0]			
BBHLCTRLB1	8406	01						R[2]			
BBLLCTRLB0	8407	00	B[2:0]		B[2:0]			G[2:0]			
BBLLCTRLB1	8408	00						R[2]			
CHSDWCTRLB0	8409	00	B[2:0]		B[2:0]			G[2:0]			
CHSDWCTRLB1	840A	00						R[2]			
reserved	840B	00									
ROMSIGCTRL	840D	00	CRS								
ROMSIGDATAB0	840E	00	CRC[7:0]								
ROMSIGDATAB1	840F	00	CRC[15:8]								
HSTRT1	8410	13	HPOS[7:0]								
VSTRT1	8411	14	VPOS[7:0]								
reserved	8412	00									
COLWIDTH1B0	8414	00	COL[7:0]								
COLWIDTH1B1	8415	00	COL[15:8]								
COLWIDTH1B2	8416	00	COL[23:16]								
COLWIDTH1B3	8417	00	COL[31:24]								
HSTRT2	8418	56	HPOS[7:0]								
VSTRT2	8419	5B	VPOS[7:0]								
W2STRTADRL	841A	00	ADDR[7:0]								
W2STRTADRH	841B	01								ADDR[8]	
										1	
COLWIDTH2B0	841C	00	COL[7:0]								
COLWIDTH2B1	841D	00	COL[15:8]								
COLWIDTH2B2	841E	00	COL[23:16]								
COLWIDTH2B3	841F	00	COL[31:24]								
BISTCONTROL	8420	00								BFAIL	BEN
BISTADDR0	8421	00	ADDR[7:0]								
BISTADDR1	8422	00								ADDR[8]	
										1	
BISTCOMPARE0	8423	00	COMPARE_DATA[7:0]								
BISTCOMPARE1	8424	00	COMPARE_DATA[11:8]								
BISTREAD0	8425	00	READ_DATA[7:0]								
BISTREAD1	8426	00	READ_DATA[11:8]								

## 3.4.5 PRE-AMP INTERFACE REGISTERS

LM1253 Pre-amp Interface Registers									
RGAINCTRL	8430	60							RGAIN[6:0]
BGAINCTRL	8431	60							BGAIN[6:0]
GGAINCTRL	8432	60							GGAIN[6:0]
CONTRCTRL	8433	30							CONTRAST[5:0]
RBIASCTRL	8434	20							RBIAS[5:0]
BBIASCTRL	8435	20							BBIAS[5:0]
GBIASCTRL	8436	20							GBIAS[5:0]
BRIGHTCTRL	8437	20							BRIGHTNESS[5:0]
DCOFFSET	8438	94		PEDESTAL[2:0]		OSD_CONT[1:0]		DC_OFFSET[2:0]	
GLOBALCTRL	8439	00						PS	BV
reserved	843A	00							
PLLFREQRNG	843E	16			IVIGAIN[1:0]		IVISTAT[1:0]		PFR[1:0]
SRTSTCTRL	843F	00	PCT	AID	TEE	MUX[1:0]		BCE	SRST

## 3.4.6 TWO-COLOR ATTRIBUTE TABLE

LM1253 Two-Color Attribute Registers									
ATT2C0n	8440 + (n*4)			C1R[1:0]		C1B[2:0]		C1G[2:0]	
ATT2C1n	+1		C2R[0]		C2B[2:0]		C2G[2:0]		C1R[2]
ATT2C2n	+2					EF[3:0]			C2R[2:1]
ATT2C3n	+3								

Two-color display character Attribute Table. The attributes for two-color display characters may be written or read via the following address format:

A15-A6: Always 1000\_0100\_01b.

A5-A2: Attribute code (0h-Fh are valid values), n

A1-A0: Determines which of the 3 bytes is to be accessed.

NOTE: In the table, n indicates the attribute number  $0 \leq n \leq 15$

NOTE: When writing, bytes 0 through 2 must be written, in that order. Bytes 0 through 2 will take effect after byte 2 is written.

Since byte 3 contains all reserved bits, this byte may be written, but no effect will result.

When reading, it is OK to read only one, two, or all three bytes.

### 3.4.7 FOUR-COLOR ATTRIBUTE TABLE

ATT4C0n	8500 +(n*8)		C1R[1:0]	C1B[2:0]	C1G[2:0]	
ATT4C1n	+1		C2R[0]	C2B[2:0]	C2G[2:0]	C1R[2]
ATT4C2n	+2			EF[3:0]		C2R[2:1]
ATT4C3n	+3					
ATT4C4n	+4		C3R[1:0]	C3B[2:0]	C3G[2:0]	
ATT4C5n	+5		C4R[0]	C4B[2:0]	C4G[2:0]	C3R[2]
ATT4C6n	+6					C4R[2:1]
ATT4C7n	+7					

Four-color display character Attribute Table. The attributes for four-color display characters may be written or read via the following address format:

A15-A7: Always 1000\_0101\_0b

A6-A3: Attribute value (0h-Fh are valid values), n

A2-A0: Determine which of the six bytes of the attribute is to be accessed.

NOTE: In the table, n indicates the attribute number,  $0 \leq n \leq 15$

NOTE: When writing, bytes 0 to 2 must be written, in that order and bytes 4 to 6 must be written, in that order.

Bytes 0 through 2 will take effect after byte 2 is written. Bytes 4 through 6 will take effect after byte 6 is written.

Since bytes 5 and 7 contain all reserved bits, these bytes may be written, but no effect will result.

When reading, it is OK to read only one, two, or all three bytes.

**THEOREM 1.**

### 3.5 DISPLAY PAGE RAM

#### 3.5.1 THE OSD WINDOW

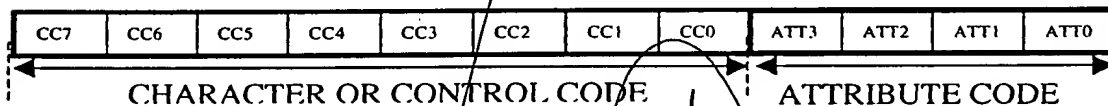
The Display Page RAM contains all of the 8 bit display character codes and their associated 4 bit attribute codes, and the special 12 bit page control codes - the row-end, skip-line parameters and window-end characters.

The LM1253 has a distinct advantage over many OSD generators that it allows variable size and format windows. The window size is not dictated by a fixed geometry area of RAM. Instead, 512 locations of 12 bit words are allocated in RAM for the definition of the windows, with special control codes to define the window size and shape.

Window width can be any length supported by the number of pixels per line that is selected divided by the number of pixels in a character line. It must be remembered that OSD characters displayed during the monitor blanking time will not be displayed on the screen, so the practical limit to the number of horizontal characters on a line is reduced by the number of characters within the horizontal blanking period.

#### 3.5.2 CHARACTER CODE AND ATTRIBUTE CODE

Each of the 512 x12 bit locations in the page RAM is comprised of an 8 bit character or control code, and a 4 bit attribute code:



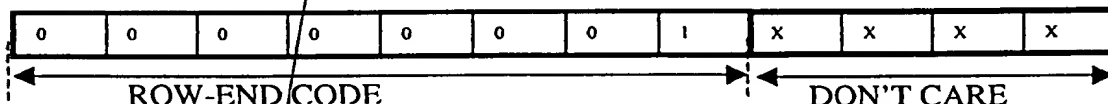
**Bits 11-4 Character Code:** These 8 bits define which of the 254 characters is to be called from the character ROM. Valid character codes are 02h - FFh.

**Bits 3-0: Attribute code:** These 4 bits address the attribute table used to specify which of the 16 locations in RAM specify the colors and enhanced features to be used for this particular character. Two separate attribute tables are used, one for 2-color characters, the other for 4-color characters.

Each of the characters are stored in sequence in the page RAM. Special codes are used between lines to show where one line ends and the next begins, and also to allow blank (or 'skipped') lines to be added between character rows.

#### 3.5.3 ROW END CODE

To signify the end of a row of characters, a special 'Row-End (RE) code is used in place of a character code.



**Bits 11-4 Row-End Code:** A special character code of 01h



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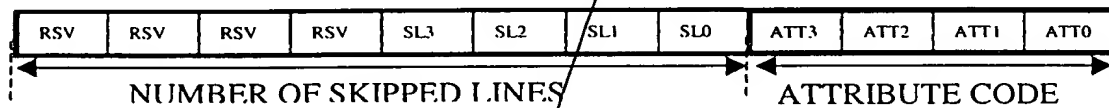
Bits 3-0: Don't care

The RE character tells the OSD generator that the character codes following must be placed on a new row in the displayed window.

### 3.5.4 SKIPPED LINE PARAMETERS

Each displayed row of characters may have up to 15 skipped (ie blank) lines beneath it in order to allow finer control of the vertical spacing of character rows. (Each skipped line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate size relative to the character cell).

To specify the number of skipped lines, the first character in each new row of characters to be displayed is interpreted differently than the other characters in the row. Instead of interpreting the data in the location as a character code, the information of the 12 bit word is defined as follows:



Bits 11-8 Reserved.

Bits 7-4: Skipped Lines. These four bits determine how many blank pixel lines will be inserted between the present row of display characters and the next row of display characters. A range of 0-15 may be selected.

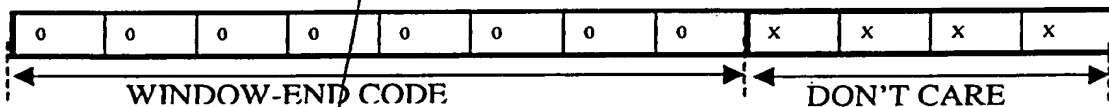
Bits 3-0: Attribute code. The pixels in the skipped lines will normally be Color 1 of the addressed 2-Color Attribute Table entry. Note that the pixels in the first line immediately below the character may be overwritten by the pixel override system that creates the button box. (Refer to the Box Formation Section for more information).

Each new line **MUST** start with an SL code, even if the number of skipped lines to follow is zero. An SL code **MUST** always follow an RE control code.

An RE code may follow an SL code if several 'transparent' lines are required between sections of the window (see example 3 below). In this case, skipped lines of zero characters are displayed, causing a break in the window.

### 3.5.5 WINDOW-END CODE

To signify the end of the window, a special 'Window-End (WE)' code is used in place of a Row-End code.



Bits 11-4 Row-End Code: A special character code of 00h

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Bits 3-0: Don't care

The WE control code tells the OSD generator that the character codes following belong to another displayed window at the next window location.

A WE control code may follow normal characters or an SL parameter, but never an RE control code.

### 3.5.6 WRITING TO THE PAGE RAM

The Display Page RAM can contain up to 512 of the above listed characters and control codes. Each character, or control code will consume one of the possible 512 locations. For convenience, a single write instruction to bit 3 of the Frame Control Register (8400h) can reset the page RAM value to all zero.

Display Window 1 will also start at the first location (corresponding to the I<sup>2</sup>C address 8000h). This location must always contain the Skip-Line (SL) parameters associated with the first row of Display Window 1. Subsequent locations should contain the characters to be displayed on row 1 of Display Window 1, until the RE character code or WE character code is written into the Display Page-RAM.

The skip-line parameters associated with the next row must always be written to the location immediately after the preceding row's row-end character. The only exception to this rule is when a window-end character (value 00h) is encountered. It is important to note that a row-end character should not precede a window-end character (otherwise the window-end character will be interpreted as the next row's skip-line parameters). Instead, the window-end character will both end the row and the window making it unnecessary to precede it with a row-end character.

The I<sup>2</sup>C Format for writing a sequence of display characters is minimized by allowing sequential characters with the same attribute code to send in a string as follows:

Byte #1 -- I<sup>2</sup>C Slave Address.

Byte #2 -- LSB Address

Byte #3 -- MSB Address

Byte #4 -- Attribute Table Entry to use for the following characters.

Byte #5 -- First display character, SL parameter, RE or WE control code.

Byte #6 -- Second display character, SL parameter, RE or WE control code.

Byte #7 -- Third display character, SL parameter, RE or WE control code.

Byte #n -- Last display character in this color sequence, SL parameter, RE or WE control code to use the associated Attribute Table Entry.

EXAMPLE #1:

### Actual On-Screen Display of Window #1:



- Every row must begin with an SL value. Display Page RAM memory location 8000h will always be associated with the SL of row 0 of Display Window #1.
- Every row except the last row of a Display Window must end with an RE character. The character immediately after an RE character is always the SL value for the next row.
- The last row in a Display Window must be a WE character. The WE character must NOT be preceded by an RE character.
- The entire Display Window may be written in a single I<sup>2</sup>C write sequence because the Attribute Table entry (ie the color palette) does not change for the entire Display Window.
- The Attribute Table Entry that associated with RE and WE characters are “don’t cares”. So in general it is most efficient just to allow them to be the same value as the Attribute Table Entry associated with the previous display character.
- The colors of the characters and background can be stored in a single location in the 2-color attribute table, in location ATT1.

Address	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh
Attribute	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1	Att1
Contents	SL'0'	C'A'	C'B'	C'C'	RE	SL'0'	C'D'	C'E'	C'F'	RE	SL'0'	C'G'	C'H'	C'I'	WE

In this example, SL is zero, as zero skipped lines are required.

### Actual On Screen Display of Window Example #2:

3 skipped lines

**Notes:**

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The contents of the display RAM are as follows:

Address	0h	1h	2h	3h	4h	05h	06h	07h	08h	09h	0Ah
Attribute	Att9	Att1	Att1	Att1	Att9	Att9	Att9	Att9	Att9	Att10	Att10
Contents	SL'3'	C'_	C'_	C'_	RE	SL'2'	C'A'	C'B'	C'C'	RE	SL'0'

Address	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h
Attribute	Att10	Att10	Att10	Att10	Att10	Att10	Att10	Att10	Att10
Contents	C'D'	C'E'	C'F'	RE	SL'3'	C'G'	C'H'	C'I'	WE

KEY: Att\_ - Attribute Table Entry. The entire Window in this example uses the same Attribute Table Entry.

**SL'n'** - Skipped Line/Parameter 'n'.

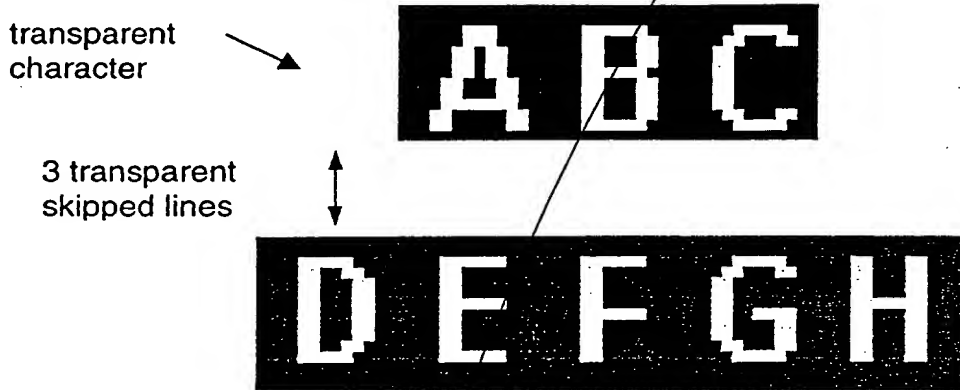
RE - Row-end Character.

**WE** - Window-end Character.

**C'\_** - Display Character value of a blank character

### EXAMPLE #3:

### Actual On Screen Display of Window Example #3:



- In order to centralize the three characters above the five characters on the row below, a 'transparent' blank character has been used as the first character on the row.
- In order to create the transparent skipped lines between the two character rows, a row of no characters has been used, resulting in a RE, SL, RE, SL control code sequence.
- In this example, the transparent lines and characters are defined by the 2-color attribute table entry ATT1. Bit 4 of Frame Control Register 1 must be set to indicate that the black color is to be translated as transparent (see section 'Control Register Definitions')
- The top row of characters are yellow on black; in this example, these are defined by the 2-color attribute table entry ATT9
- The second row of characters are blue on black; in this example, these are defined by the 2-color attribute table entry ATT10

The contents of the display RAM are as follows:

## LM1253 PREAMP+ OSD GENERATOR: V0.1

AG<sup>2</sup>DC

Address	0h	1h	06h	07h	08h	09h	0Ah	09h	0Ah
Attribute	Att1	Att1	Att9	Att9	Att9	Att9	Att1	Att10	Att10
Contents	SL'0'	C'_'	C'A'	C'B'	C'C'	RE	SL'3'	RE	SL'0'

Address	0Bh	0Ch	0Dh	10h	11h	13h
Attribute	Att10	Att10	Att10	Att10	Att10	Att10
Contents	C'D'	C'E'	C'F'	C'G'	C'H'	WE

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**3.6 CONTROL REGISTER DEFINITIONS****Frame Control Register 1 (I<sup>2</sup>C address 8400h).****REGISTER NAME: FRMCTRL1**

Bit 7 Bit 0

RSV	RSV	RSV	TE	CDPR	D2E	D1E	OsE
-----	-----	-----	----	------	-----	-----	-----

Bit 0: On-Screen Display Enable. The On-Screen Display will be disabled when this bit is a zero. When this bit is a one the On-Screen Display will be enabled and Display Window 1 will be enabled if Bit 1 of this register is a one; likewise Display Window 2 will be enabled if Bit 2 of this register is a one.

Bit 1: Display Window 1 Enable. When Bit 0 of this register and this bit are both ones, Display Window 1 is enabled. If either bit is a zero, then Display Window 1 will be disabled.

Bit 2: Display Window 2 Enable. When Bit 0 of this register and this bit are both ones, Display Window 2 is enabled. If either bit is a zero, then Display Window 2 will be disabled.

Bit 3: Clear Display Page RAM. Writing a one to this bit will result in setting all of the Display Page RAM values to zero. This bit is automatically cleared after the operation is complete.

Bit 4: Transparent Disable. When this bit is a zero, a palette color of black (ie color palette look-up table value of '000 000 000') in Color 1 of the first 8 palette look-up table address locations (ie ATT = 0h-7h) will be translated as transparent. When this bit is a one, the color will be translated as black.

Bits 7-4: RESERVED.



Frame Control Register 2 (I<sup>2</sup>C address 8401h).

REGISTER NAME: FRMCTRL2

Bit 7 Bit 0

PL2	PL1	PL0	BP4	BP3	BP2	BP1	BP0
-----	-----	-----	-----	-----	-----	-----	-----

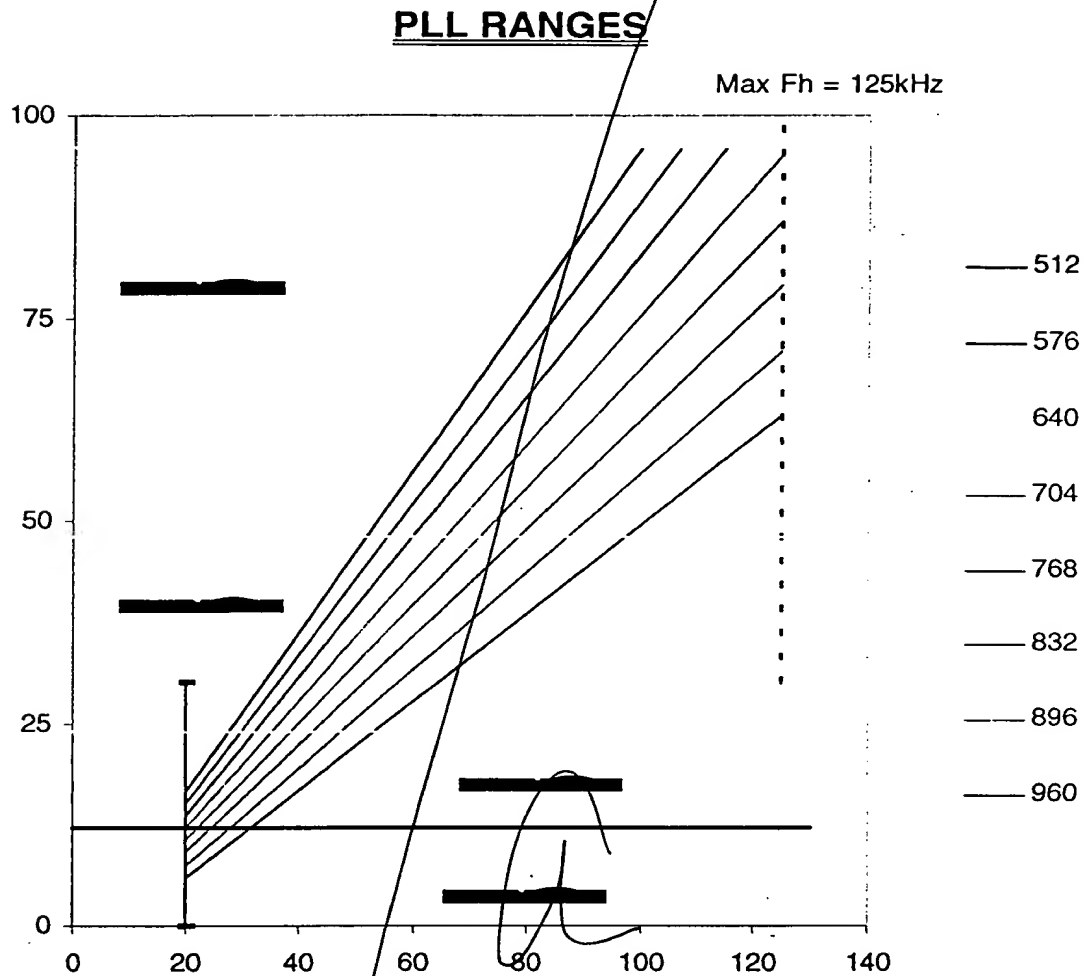
Bit 4-0: Blinking Period. These five bits set the blinking period of the blinking feature., which is determined by multiplying the value of these bits by 8, and then multiplying the result by the vertical field rate.

Bits 7-5: Pixels per Line. These three bits determine the number of Pixels per line.

Bits 5-3	Description	Max Fh
000b	512 pixels per line	125kHz
001b	576 pixels per line	125kHz
010b	640 pixels per line	125kHz
011b	704 pixels per line	125kHz
100b	768 pixels per line	125kHz
101b	832 pixels per line	115kHz
110b	896 pixels per line	107kHz
111b	960 pixels per line	100kHz

Bits 7-6: RESERVED.

Note: the pixels per line must be set in conjunction with the PLL lock range as per the figure below. Note that the maximum horizontal frequency of the three highest resolutions is limited.



Character Font Access Control Register (I<sup>2</sup>C address 8402h).

REGISTER NAME: CHARFONTACC

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	C/A	Bit
-----	-----	-----	-----	-----	-----	-----	-----

Bit 0: Four-color pixel data value Bit indicator. This bit indicates if Bit 0 (when a zero) or Bit 1 (when a one) of the four-color pixel data value is being accessed via I2C addresses 3000h – 3FFFh.

Bit 1: Character/Attribute Code Indicator. This bit controls what value is read via I2C reads of the Display Page RAM (address range 8000h-81FFh). When this bit is a 0, such reads will return the character code. When this bit is a 1, the attribute code will be returned.

Bits 7-2: RESERVED.

### Vertical Blank Duration Control Register (I<sup>2</sup>C address 8403h).

#### REGISTER NAME: VBLANKDUR

Bit 7 Bit 0

RSV	VB6	VB5	VB4	VB3	VB2	VB1	VB0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 6-0: Vertical Blank Duration. These seven bits set the duration of the VBLANK signal in numbers of horizontal scan lines.

Bit 7: RESERVED.

### OSD Character Height Control Register (I<sup>2</sup>C address 8404h).

#### REGISTER NAME: CHARHTCTRL

Bit 7 Bit 0

CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
-----	-----	-----	-----	-----	-----	-----	-----

Bit 7-0: Character Height: this register sets the character height according to the constant character height mechanism described in section Constant Character Height Mechanism. The value programmed in the register is equal to the approximate number of OSD height compensated lines required on the screen divided by 4. The value is only approximate, due to the approximation used in scaling the characters.

Example: If approximately 384 OSD lines are required on the screen (regardless of the number of image lines) then the Character Height Control Register is programmed with the value of 81.

### Button Box Highlight Color Register (EF1) (I<sup>2</sup>C address 8405h-8406h).

#### REGISTER NAME: BBHLCTRLB1 (8406h) BBHLCTRLB0 (8405h)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	R2	R1	R0	B2	B1	B0	G2	G1	G0
-----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----

Bits 8-0: Button Box highlight color. This register indicates the value of Enhanced Feature (button box highlight) register EF1.

Bits 15-9: RESERVED.

**Button Box Lowlight Color Register (EF2) (I<sup>2</sup>C address 8407h-8408h).****REGISTER NAME: BLLCTRLB1 (8408h) BLLCTRLB0 (8407h)**

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	R2	R1	R0	B2	B1	B0	G2	G1	G0
-----	-----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----

Bits 8-0: Button Box lowlight color. This register indicates the value of Enhanced Feature (button box lowlight) register EF2.

Bits 15-9: RESERVED.

**Heavy Button Box Lowlight / Shadow /Shading Color Register (EF3) (I<sup>2</sup>C address 8409h-840Ah).****REGISTER NAME: CHSDWCTRLB1 (840Ah) CHSDWCTRLB0 (8409h)**

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	R2	R1	R0	B2	B1	B0	G2	G1	G0
-----	-----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----

Bits 8-0: Heavy Button Box lowlight /shadow color. This register indicates the value of Enhanced Feature (heavy button box lowlight or shadow/shading) register EF3.

Bits 15-9: RESERVED.

**ROM Signature Control Register (I<sup>2</sup>C address 840Dh).****REGISTER NAME: ROMSIGCTRL**

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	CRS
-----	-----	-----	-----	-----	-----	-----	-----	-----

Bit 0: Calculate ROM Signature. Setting this bit causes the entire ROM to be read, sequentially, and a 16 bit CRC calculated over its contents. The residual value from this calculation is placed in the ROM Signature Data register. This bit automatically clears itself when the calculation has been completed.

Bits 7-1: RESERVED.

**ROM Signature Data Register (I<sup>2</sup>C address 840Eh-840Fh).****REGISTER NAME: ROMSIGDATAB1 (840Fh) ROMSIGDATAB0 (840Eh)**

Bit 15 Bit 8 Bit 7 Bit 0

CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
-------	-------	-------	-------	-------	-------	------	------	------	------	------	------	------	------	------	------

Bits 15-0: ROM Signature Data. This register indicates the residual value from the

CRC calculation. Devices containing ROMs with different programming will give different signatures. Devices with the same ROM programming will give the same signature.

### Display Window 1 Horizontal Pixel Start Location Register (I<sup>2</sup>C address 8410h).

**REGISTER NAME: HSTRT1 (8410h)**

Bit 7 Bit 0

1H7	1H6	1H5	1H4	1H3	1H2	1H1	1H0
-----	-----	-----	-----	-----	-----	-----	-----

Bit 7-0: Display Window 1 Horizontal Pixel Start Location. These seven bits determine the starting horizontal pixel location, which is determined by multiplying the value of these bits by 4 and adding 30 pixels. Due to pipeline delays, the first usable location for the OSD window is approx 42 pixels to the right of the horizontal flyback pulse. For this reason, the display start location must be programmed with a number larger than 2, otherwise improper operation may occur.

### Display Window 1 Vertical Pixel Start Location Register (I<sup>2</sup>C address 8411h).

**REGISTER NAME: VSTRT1 (8411h)**

Bit 7 Bit 0

1V7	1V6	1V5	1V4	1V3	1V2	1V1	1V0
-----	-----	-----	-----	-----	-----	-----	-----

Bit 7-0: Display Window 1 Vertical Pixel Start Location. These eight bits determine the starting vertical pixel location in constant height character lines, which is determined by multiplying the value of these bits by 2. (Note, each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the character cell size – see section Constant Character Height Mechanism).

### Display Window 1 Column Width Control Register (I<sup>2</sup>C address 8414h-8417h).

**REGISTER NAME: COLWIDTH1B3 (8417h) COLWIDTH1B2 (8416h) COLWIDTH1B1 (8415h) COLWIDTH1B0 (8414h)**

Bit 31 Bit 16

COL31	COL30	COL29	COL28	COL27	COL26	COL25	COL24	COL23	COL22	COL21	COL20	COL19	COL18	CRC17	COL16
-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------

Bit 15 Bit 0

COL15	COL14	COL13	COL12	COL11	COL10	COL9	COL8	COL7	COL6	COL5	COL4	COL3	COL2	COL1	COL0
-------	-------	-------	-------	-------	-------	------	------	------	------	------	------	------	------	------	------

Bits 31-0: Display Window 1 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31-0 of Display Window 1, respectively. A value of zero indicates the column will have normal width (12 pixels). A value of one indicates the

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column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations.

The user should note that if more than 32 display characters are programmed to reside on a row, then all display characters after the first thirty-two will have normal width (12 pixels).

### Display Window 2 Horizontal Pixel Start Location Register (I<sup>2</sup>C address 8418h).

REGISTER NAME: HSTRT2 (8418h)

Bit 7 Bit 0

2H7	2H6	2H5	2H4	2H3	2H2	2H1	2H0
-----	-----	-----	-----	-----	-----	-----	-----

Bit 7-0: Display Window 2 Horizontal Pixel Start Location. These seven bits determine the starting horizontal pixel location, which is determined by multiplying the value of these bits by 4.

### Display Window 2 Vertical Pixel Start Location Register (I<sup>2</sup>C address 8419h).

REGISTER NAME: VSTRT2 (8419h)

Bit 7 Bit 0

2V7	2V6	2V5	2V4	2V3	2V2	2V1	2V0
-----	-----	-----	-----	-----	-----	-----	-----

Bit 7-0: Display Window 2 Vertical Pixel Start Location. These eight bits determine the starting vertical pixel location in constant height character lines, which is determined by multiplying the value of these bits by 2. (Note, each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the character cell size – see section Constant Character Height Mechanism).

### Display Window 2 Starting Address in the Display Page RAM (I<sup>2</sup>C address 841Ah-841Bh).

REGISTER NAME: W2STRTADRH (841Bh) W2STRTADRL (841Ah)

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	2a8	2a7	2a6	2a5	2a4	2a3	2a2	2a1	2a0
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

Bits 8-0: Display Window 2's Starting Address in the Display Page RAM. This register determines the starting address of Display Window 2 in the Display Page RAM. This first address location will always contain the SL code for the first row of Display Window 2.

Bits 7-5: RESERVED.

**Display Window 2 Column Width Control Register (I<sup>2</sup>C address 841Ch-841Fh).****REGISTER NAME: COLWIDTH2B3 (841Fh) COLWIDTH2B2 (841Eh) COLWIDTH2B1 (841Dh) COLWIDTH2B0 (841Ch)**

Bit 31 Bit 24 Bit 23 Bit 16

COL31	COL30	COL29	COL28	COL27	COL26	COL25	COL24	COL23	COL22	COL21	COL20	COL19	COL18	CRC17	COL16
-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------	-------

Bit 15 Bit 8 Bit 7 Bit 0

COL15	COL14	COL13	COL12	COL11	COL10	COL9	COL8	COL7	COL6	COL5	COL4	COL3	COL2	COL1	COL0
-------	-------	-------	-------	-------	-------	------	------	------	------	------	------	------	------	------	------

Bits 31-0: Display Window 2 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31-0 of Display Window 2, respectively. A value of zero indicates the column will have normal width (12 pixels). A value of one indicates the column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations.

The user should note that if more than 32 display characters are programmed to reside on a row, then all display characters after the first thirty-two will have normal width (12 pixels).

**Built In Self Test Control Register (I<sup>2</sup>C address 8420h).****REGISTER NAME: BISTCONTROL (8420h)**

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	BFAIL	BEN
-----	-----	-----	-----	-----	-----	-------	-----

Bit 0: BIST Enable (BEN). Setting this bit causes the RAM built-in self test to be performed. This bit automatically clears itself when the test has completed.

Bit 1: BIST Fail (BFAIL). This bit indicates the results of the RAM built-in self test. After completion of the test, a 1 in this bit indicates a failure, and a 0 indicates success.

Bit 7-2: Reserved

**Built In Self Test Address Register (I<sup>2</sup>C address 8421-8422h).****REGISTER NAME: BISTADDR1 (8422h) BISTADDR0 (8421h)**

Bit 15 Bit 8 Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	ADDR8	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
-----	-----	-----	-----	-----	-----	-----	-----	-------	-------	-------	-------	-------	-------	-------	-------	-------

Bits 8-0: Address (ADDR). These bits indicate address of the first failing location





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**Green Channel Gain Control Register (I<sup>2</sup>C address 8432h).****REGISTER NAME: GGAINCTRL (8432h)**

Bit 7 Bit 0

RSV	GG6	GG5	GG4	GG3	GG2	GG1	GG0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 6-0: Green Channel Gain Control. These seven bits determine the gain for the Green Channel.

Bit 7: RESERVED.

**Contrast Control Register (I<sup>2</sup>C address 8433h).****REGISTER NAME: CONTRCTRL (8433h)**

Bit 7 Bit 0

RSV	RSV	CG5	CG4	CG3	CG2	CG1	CG0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 5-0: Contrast Gain Control. These six bits determine the overall gain of all three channels.

Bits 7-6: RESERVED.

**Red Bias Clamp Pulse Amplitude Control Register (I<sup>2</sup>C address 8434h).****REGISTER NAME: RBIASCTRL (8434h)**

Bit 7 Bit 0

RSV	RSV	RC5	RC4	RC3	RC2	RC1	RC0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 5-0: Red Channel Bias Clamp Pulse Amplitude Control. These six bits determine the bias clamp value for its pulse amplitude.

Bits 7-6: RESERVED.

**Blue Bias Clamp Pulse Amplitude Control Register (I<sup>2</sup>C address 8435h).****REGISTER NAME: BBIASCTRL (8435h)**

Bit 7 Bit 0

RSV	RSV	BC5	BC4	BC3	BC2	BC1	BC0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 5-0: Blue Channel Bias Clamp Pulse Amplitude Control. These six bits determine the bias clamp value for its pulse amplitude.

Bits 7-6: RESERVED.

**Green Bias Clamp Pulse Amplitude Control Register (I<sup>2</sup>C address 8436h).****REGISTER NAME: GBIASCTRL (8436h)**

Bit 7 Bit 0

RSV	RSV	GC5	GC4	GC3	GC2	GC1	GC0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 5-0: Green Channel Bias Clamp Pulse Amplitude Control. These six bits determine the bias clamp value for its pulse amplitude.

Bits 7-6: RESERVED.

**Brightness Amplitude Control Register (I<sup>2</sup>C address 8437h).****REGISTER NAME: BRIGHTCTRL (8437h)**

Bit 7 Bit 0

RSV	RSV	BA5	BA4	BA3	BA2	BA1	BA0
-----	-----	-----	-----	-----	-----	-----	-----

Bits 5-0: Brightness Amplitude Control. These six bits determine the amplitude of brightness for all three channels.

Bits 7-6: RESERVED.

**DC Offset and OSD Contrast Control Register (I<sup>2</sup>C address 8438h).****REGISTER NAME: DCOFFSET (8438h)**

Bit 7 Bit 0

BP2	BP1	BP0	OSD C1	OSD C0	DC2	DC1	DC0
-----	-----	-----	-----------	-----------	-----	-----	-----

Bits 2-0: DC Offset Control. These three bits determine the active video DC offset to all three channels.

Bits 4-3: OSD Contrast. These two bits determine the OSD contrast.

Bits 7-5: Blanking pedestal. These three bits determine the blanking pedestal offset for all three channels.

**Global Video Control Register (I<sup>2</sup>C address 8439h).****REGISTER NAME: GLOBALCTRL (8439h)**

Bit 7 Bit 0

RSV	RSV	RSV	RSV	RSV	RSV	PS	BV
-----	-----	-----	-----	-----	-----	----	----

Bit 0: Blank Video. When this bit is a one, blank the video output. When this bit is a zero allow normal video out.

Bit 1: Power Save. When this bit is a one, shut down the analog circuits to support

sleep mode. When this bit is a zero enable the analog/circuits for normal operation.

Bits 7-2: RESERVED.

### PLL Frequency Range Control Register (I<sup>2</sup>C address 843Eh).

**REGISTER NAME: PLLFREQRNG (843Eh)**

Bit 7    Bit 0

RSV	RSV	IVIG1	IVIG0	IVS1	IVS0	PFR1	PFR0
-----	-----	-------	-------	------	------	------	------

Bit 1-0: PLL Frequency Range Control. These bits assist the PLL in locking to the desired pixel frequency. They are set based upon the desired pixel frequency range as follows:

00b if desired OSD pixel frequency is between 6MHz and 12MHz

01b if desired OSD pixel frequency is between 12MHz and 24MHz

10b if desired OSD pixel frequency is between 24MHz and 48MHz

11b if desired OSD pixel frequency is between 48MHz and 96MHz

Bits 3-2: IVISTAT. These bits control the minimum current of the V to I block of the PLL. The normal value of these bits is 01. These will not normally be altered by the user.

Bits 5-4: IVIGAIN. These bits control the gain of the V to I block of the PLL. The normal value of these bits is 01. These will not normally be altered by the user.

The PLL range should be set according to the table below:

PIXEL MODE	RANGE 0	RANGE 1	RANGE 2	RANGE 3
512	20-38	36-48	46-95	92-125
576	20-22	20-42	40-84	81-125
640	NA	20-39	37-76	73-125
704	NA	20-35	33-69	66-125
768	NA	20-32	30-64	61-125
832	NA	20-30	28-58	55-115
896	NA	20-28	26-54	52-107
960	NA	20-26	24-50	48-100

As IVIGAIN and IVISTAT are not normally changed by the user, the PLL Frequency Control Register should normally be written with the following values, depending upon the range of operation required:

RANGE 0	RANGE 1	RANGE 2	RANGE 3
14h	15h	16h	17h

### Software Reset and Test Control Register (I<sup>2</sup>C address 843Fh).

**REGISTER NAME: SRTSTCTRL (843Fh)**

Bit 7    Bit 0

PCT	AID	TEE	MUX1	MUX0	BCE	RSV	SRST
-----	-----	-----	------	------	-----	-----	------

Bit 0: Software Reset. Setting this bit causes a software reset. All registers (except this one) are loaded with their default values. All operations currently in progress are aborted (except for I2C transactions). This bit automatically clears itself when the reset has been completed.

**Bit 1: Reserved**

Bit 2: Bypass Clock Enable. Setting this bit deselects the PLL as the source of the pixel clock, and selects the ABL input as the source of the pixel clock.

Bits 4-3: Multiplexed Output Select (MUX). Setting these bits selects which signal will be routed to the SCL output when test mode is enabled.

- 00 selects static LOW output  
01 selects Pixel Clock from PLL  
10 selects POWERGOOD signal from Power Quality Monitor  
11 selects Horizontal rate feedback signal from PLL

**Bit 5: Test Enable Enable.** Setting this bit enables the CLAMP input to be used as a Test Enable input.

**Bit 6: Auto Increment Disable.** Setting this bit disables the automatic address increment feature of the I2C register access protocol. With this bit set, any I2C register may be continuously read or written without sending its address between register accesses.

**Bit 7: Parallel Channel Test.** Setting this bit causes the Red channel controls to apply to the Blue and Green channels, enabling ramp testing to be done in parallel on all 3 channels.

### 3.6.2 ATTRIBUTE TABLE AND ENHANCED FEATURES

Each display character and SL in the Display Page RAM will have a 4-bit Attribute Table entry associated with it. The user should note that two-color display characters and four-color display characters use two different Attribute Tables, effectively providing 16 attributes for two-color display characters and 16 attributes for four-color display characters.

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For two-color characters the attribute contains the code for the 9-bit foreground color (Color 2), the code for the 9-bit background color (Color 1), and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, bordering, etc.).

For four-color characters the attribute contains the code for the 9-bit Color 1, the code for the 9-bit Color 2, the code for the 9-bit Color 3, the code for the 9-bit Color 4 and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, bordering, etc.).

### 3.6.3 TWO-COLOR ATTRIBUTE FORMAT

**REGISTER NAME:** ATT2C3n (8443h +(n\*4)), ATT2C2n (8442h +(n\*4)),  
where n = attribute code

Bit 31 Bit 24 Bit 23 Bit 16

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EFB3	EFB2	EFB1	EFB0	C2R2	C2R1
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

**REGISTER NAME:** ATT2C1n (8441h +(n\*4)), ATT2C0n (8440h +(n\*4)),  
where n = attribute code

Bit 15 Bit 8 Bit 7 Bit 0

C2R0	C2B2	C2B1	C2B0	C2G2	C2G1	C2G0	C1R2	C1R1	C1R0	C1B2	C1B1	C1B0	C1G2	C1G1	C1G0
------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------

Bits 8-0: Color 1. These nine bits indicate the value of the color to be displayed as color 1. This is considered to be the background color and is displayed when the corresponding pixel data bit is a zero.

Bits 17-9: Color 2. These nine bits indicate the value of the color to be displayed as color 2. This is considered to be the foreground color and is displayed when the corresponding pixel data bit is a one.

Bits 21-18: Enhanced Feature Bits. The enhanced features are determined as follows:

**Bits 31-24: Reserved**



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## 3.6.4 FOUR-COLOR ATTRIBUTE FORMAT

**REGISTER NAME:** ATT4C7n (8507h +(n\*4)), ATT4C6n (8506h +(n\*4)),  
 where n = attribute cod

Bit 63 Bit 56      Bit 55 Bit 48

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	C4R2	C4R1
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------

**REGISTER NAME:** ATT4C5n (8505h +(n\*4)), ATT4C4n (8504h +(n\*4)),  
 where n = attribute code

Bit 47 Bit 40      Bit 39 Bit 32

C4R0	C4B2	C4B1	C4B0	C4G2	C4G1	C4G0	C3R2	C3R1	C3R0	C3B2	C3B1	C3B0	C3G2	C3G1	C3G0
------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------

**REGISTER NAME:** ATT4C3n (8503h +(n\*4)), ATT4C2n (8502h +(n\*4)),  
 where n = attribute code

Bit 31 Bit 24      Bit 23 Bit 16

RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	EFB3	EFB2	EFB1	EFB0	C2R2	C2R1
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

**REGISTER NAME:** ATT4C1n (8501h +(n\*4)), ATT4C0n (8500h +(n\*4)),  
 where n = attribute code

Bit 15 Bit 8      Bit 7 Bit 0

C2R0	C2B2	C2B1	C2B0	C2G2	C2G1	C2G0	C1R2	C1R1	C1R0	C1B2	C1B1	C1B0	C1G2	C1G1	C1G0
------	------	------	------	------	------	------	------	------	------	------	------	------	------	------	------

Bits 8-0: Color 1. These nine bits indicate the value of the color to be displayed as color1. This is considered to be the background color and is displayed when the corresponding pixel data bit is 00b

Bits 17-9: Color 2. These nine bits indicate the value of the color to be displayed as color2. This is displayed when the corresponding pixel data bit is 01b

Bits 21-18: Enhanced Feature Bits. The enhanced features are determined as follows:

<u>Bits 21-18</u>	<u>Description</u>
0000b	Normal (no enhanced features enabled).
0001b	Blinking.
001Xb	RESERVED.
01XXb	RESERVED.
1000b	Raised Box.
1001b	Blinking and Raised Box.
1010b	Depressed Box.
1011b	Blinking and Depressed Box.
1100b	Heavy Raised Box.
1101b	Blinking and Heavy Raised Box.
1110b	Heavy Depressed Box.
1111b	Blinking and Heavy Depressed Box.

Bits 40-32: Color3. These nine bits indicate the value of the color to be displayed as color3. This is displayed when the corresponding pixel data bit is 10b.

Bits 49-41: Color4. These nine bits indicate the value of the color to be displayed as color4. This is displayed when the corresponding pixel data bit is 11b.

Bits 63-50: RESERVED.



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8530h-  
8538h-  
8542h-

~~WORK FOR~~  
~~most sig~~  
~~bottom~~  
~~, and~~  
~~- NO~~

~~WORK FOR~~  
~~most sig~~  
~~bottom~~  
~~, and~~  
~~- NO~~

Boxes are created by a 'pixel override' system that overwrites character cell pixel information with either the highlight color (EF1) or low light shadow (EF2 or EF3) of the box. Only the top pixel line of the character and the right edge of the character can be overwritten by the pixel override system.

The bottom edge of a box is created by either

- Or:

- overwriting the pixels in the top line of the skipped lines below, in the case where skip lines are present below a boxed character.

on whether

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# INVESTIGATION

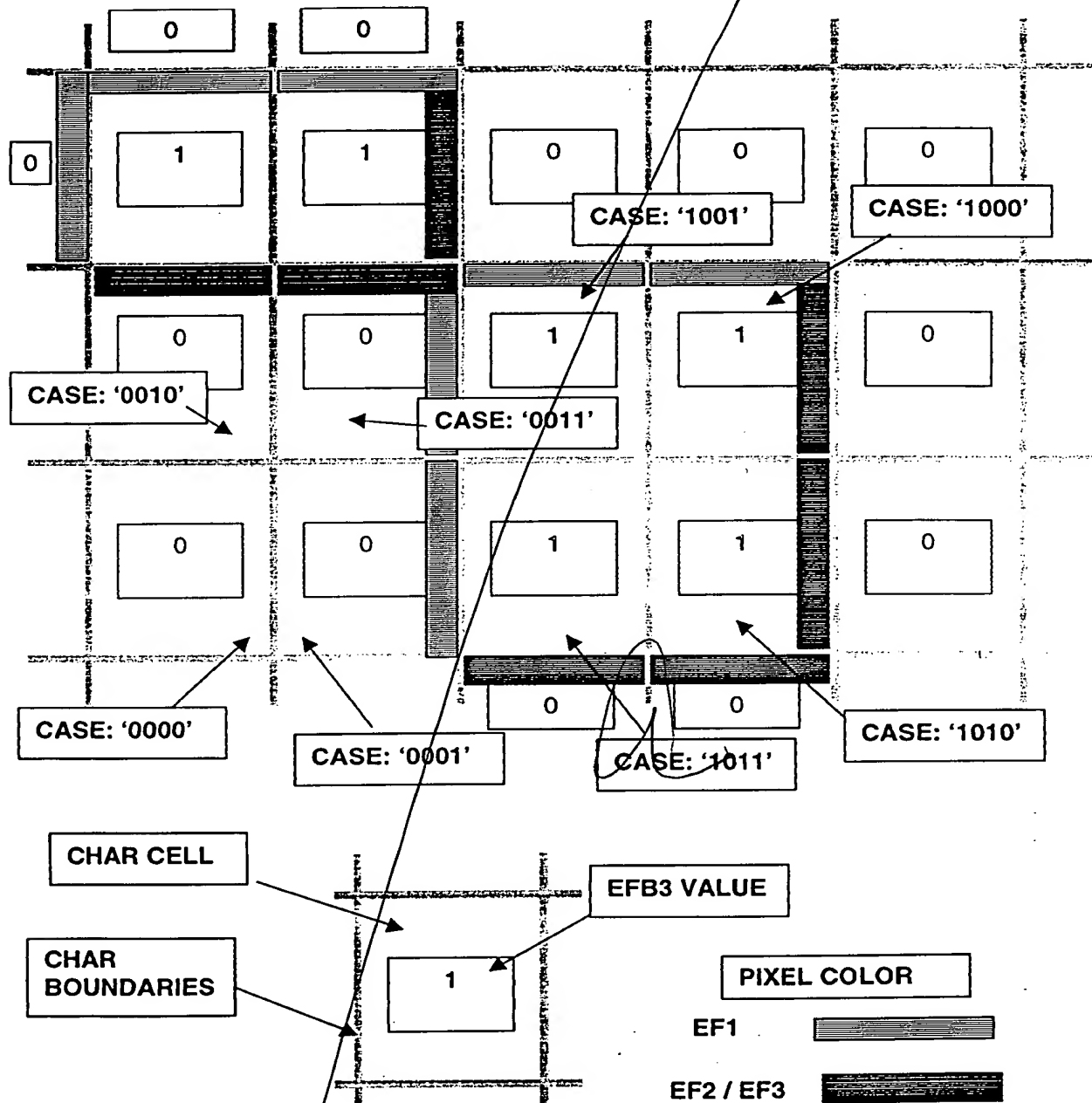


Figure 25 BUTTON BOX CONSTRUCTION (NO SKIP LINES)

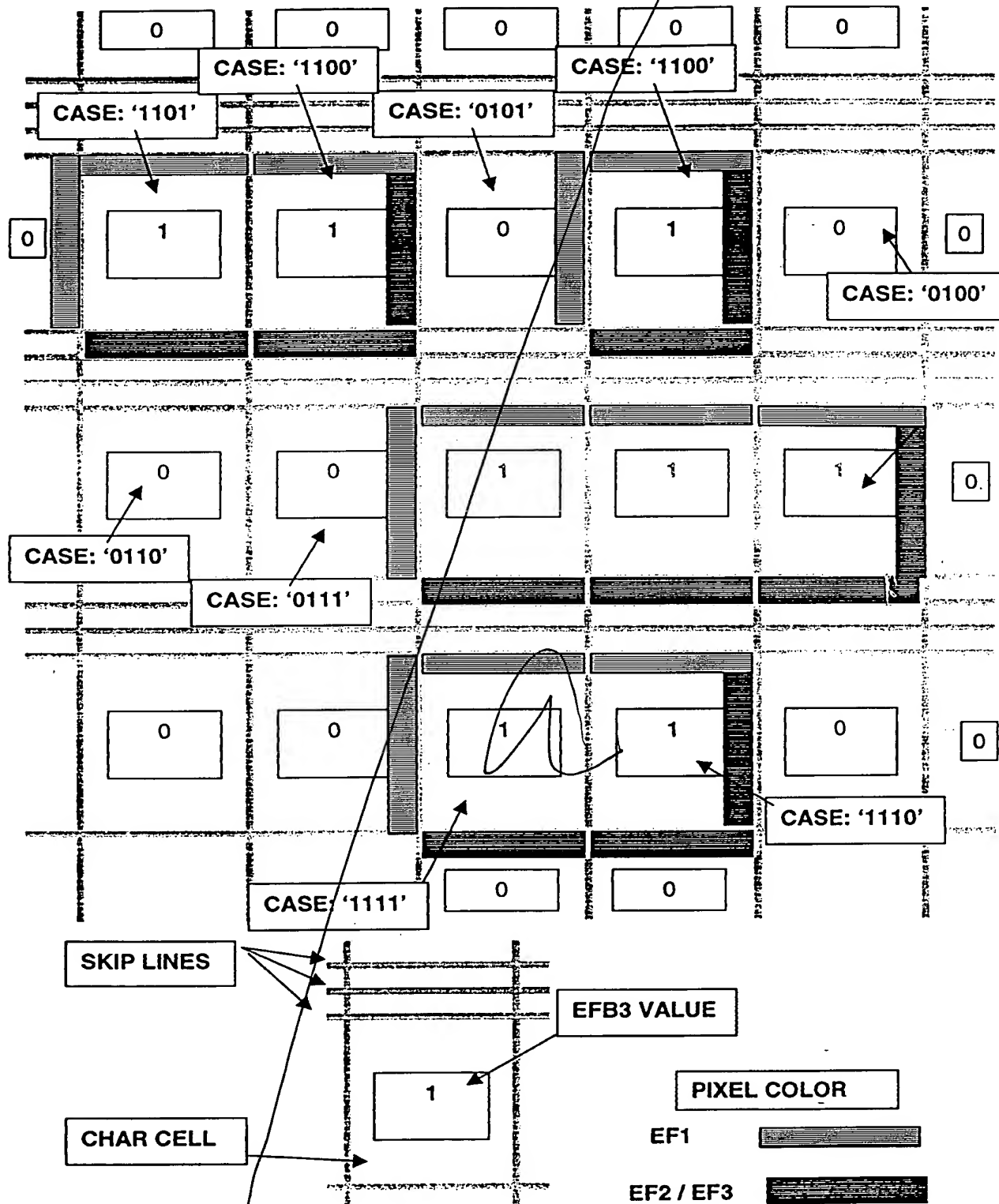


Figure 26 BUTTON BOX CONSTRUCTION (WITH SKIP LINES)

- No box may use the left most display character in the Display Window, or it will have no left side of the Box. To create a box around the left most displayed character, a transparent 'blank' character must be used in the first character position. This character will not be visible on the screen, but allows the formation of the box.
- At least one skip line must be used beneath characters on the bottom row, if a box is required around any characters on this row in order to accommodate the bottom edge of the box.
- Skipped lines cannot be used within a box covering several rows
- Irregular shaped boxes, (ie other than rectangular), may have some missing edges.

### Figure 27 OPERATION OF THE SHADOW FEATURE

Because the shadowing relies upon information about the pixels surrounding any given pixel, the bordering system may not operate correctly for pixels in line 0, line 17, and column 0 and column 11.

### 3.7 CONSTANT CHARACTER HEIGHT MECHANISM

The CRT monitor scan circuits ensure that the height of the displayed image remains the constant, and so the physical height of a single displayed pixel row will decrease as the total number of vertical image lines increases. If the OSD character matrix has a fixed number of lines,  $C$ , (where  $C=16$ ), then the character height will reduce as the number of scan lines increase, assuming a constant image height. To prevent this, the OSD generator repeats some of the lines in the OSD character in order to maintain a constant height.

The constant character height mechanism detects when interlace mode is being used and compensates to ensure the character height remains the same as for non-interlaced formats.

### 3.8 DISPLAY WINDOW1 TO DISPLAY WINDOW2 SPACING

There is no required vertical spacing between Display Window 1 and Display Window 2, but they should not overlap.

There must be a two character horizontal space between Display Window 1 and Display Window 2 for proper operation of both windows or undefined results may occur.

## 4 EVALUATION CHARACTER FONTS

The preliminary character font for evaluation of the LM1253 is shown in the figures below.

Also note that the first two character codes of the two color font (00h and 01h) are reserved for the Window End (WE) and Row End (RE) codes respectively.



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00h

1Fh

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z				
a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z				
1	2	3	4	5	6	7	8	9	0	=	!	@	#	\$	%	&	*	(	)	-	+	:	;	'	'	'	'	'	'
.	>	<	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	
?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

E0h

FFh

Figure 28 EVALUATION CHARACTER FONT